380Z
SERVICE MANUAL

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380Z AND 480Z SYSTEMS

SERVICE MANUAL

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SECTION 1

CPU BOARD

INTRODUCTION

This section describes the circuitry of the CPU board supporting COS versions 3.0, 3.4 and 4.0. There is no hardware alteration between the three COS version CPU boards, although differences do exist on boards supporting COS 2.3 or earlier. No attempt is made to document these early boards as so few are now in use.

CIRCUIT DESCRIPTION

(Circuit: 380Z : CPU/RAM
380Z : CPU-2)

The CPU board incorporates:

- a Z80-A processor
- processor support
- bus control/buffering
- two fully supported 16K banks of dynamic RAM
- space for three 2716/2708 monitor EPROMS (fully supported)
- system clock
- an 8-bit parallel bi-directional port (user port).

Processor and Processor Support

(Circuit 380Z : CPU-2)

The Z80A processor is clocked at 4MHz from the system clock. Interrupt request sequences are not used by the operating system, but the 50-way bus allows for external interrupts to be serviced (J3-30). Bus Request/Acknowledge (Req/Ack) sequences are not used by the operating system, but, again, the 50-way bus allows for future expansion (DMA etc.).

Non-maskable interrupt (NMI) routines are used by the operating system to service the "single-step" Front Panel command. NMIEN- is derived from a bit in system port 0 on the VDU board, which then enables counter IC 1 (LS90). On the eighth M1 cycle after NMIEN- becomes active 'low', an active 'high' output from the counter is inverted to produce active 'low' NMI-. During this period, NMIEN- must be disabled within eight M1 cycles or else NMI is activated again and a loop is established. The repetition of NMI requests is a very common fault condition associated with "garbage" on the screen.

After a processor reset, system port 0 is cleared and NMIEN- is active. EPROM 0 is mapped to address 0000H-0800H on page 0 where instructions are located within the first two M1 cycles to initialize system port 0 and prevent NMI. If these instructions are not executed, due to a fault condition, the repeated NMI results in a loop in which the screen is not cleared and "garbage" is displayed.

The reset circuitry lies mainly on the VDU board where a 2400Hz signal is synchronized with the M1 cycle so that the processor only receives active 'low' reset during M1 cycles. This ensures that RAM contents are not corrupted during reset. In the absence of reset, due to a CPU board fault (which usually results in "garbage"), M1 should toggle to enable reset pulses on the VDU board (power-on reset excluded).

When power is applied to the Z80, M1 is inactive until the processor is reset. Absence of power on 'reset' reaching the processor will normally result in inactive M1 and no response to the RESET button. The situation can be very "Catch 22" if this is not borne in mind when tackling faults around this circuitry. Bus reset is buffered by a transistor to drive the bus; processor reset is inverted by a segment of IC 20 to drive pin 26 of the Z80A CPU.

One wait cycle is inserted every memory cycle in the following way: on the first rising edge of the system clock, after MRQ- becomes active 'low' (start of memory cycle), MRQ- is clocked through D-type flip-flop IC 22 and appears as a 'high' on the Q-output (pin 8). One system clock cycle later it appears, as a 'low' on the Q-output pin 5. Both outputs are then NANDed by IC 20. The output of IC 20 is WAIT- and is exactly one system clock cycle in duration with a delayed (one clock cycle) inverted version of itself produced in the other half of IC 22. The output of IC 20 pin 13 is WAIT- and is exactly one clock cycle in duration.

In the absence of interrupt requests, and if the HALT- output of the processor is active 'low', the processor has executed a halt command: the system will be irretrievably locked, and can only be restarted by an external interrupt or system reset. HALT- is available on the 50-way bus for future expansion.

To produce the signal NOT(M1+RD), two high-speed diodes are used in a diode resistor AND gate to minimize propagation delay. The signal is used to select the direction of transfer of data through bi-directional tristate buffers, ICs 14 and 15 (74LS241).

Bus Control and Buffering

(Circuit 380Z : CPU-2)

Apart from processor control signals, the main bus can be divided into two sections:

- An 8-bit bi-directional data bus (BD0-BD7)
- A 16-bit uni-directional address bus (BA0-BA15).

The data bus is buffered from the processor by ICs 14 and 15. All 8 bits

are transferred directly to the 50-way bus (J3 3-10) and the 37-way bus to the VDU board (J2 16-23). With the exception of external bus Request/Acknowledge cycles, the processor controls the direction of transfer of data in the bus, as described under 'Processor Support', above. In response to an interrupt request M1- can occur without RD- during data transfer to the Z80, so it is necessary to control the bus direction by using the ORed function of M1- and RD-. All devices which drive the data bus have tristate output stages.

The address bus is buffered from the processor by ICs 8, 9, and 10. All 16 bits are transferred directly to the 50-way bus (J3 11-26) and the least significant 11 bits (BA0-BA10) are transferred to the VDU board via the 34-way bus (J2 24-34). With the exception of external bus Request/Acknowledge cycles, the processor drives the bus exclusively, and the address buffers are constantly enabled.

EPROM and EPROM Support

(Circuit 380Z : CPU-2)

There are three 24-pin sockets on the CPU board so that either 2716 or 2708 EPROMS (by link connections) can function in any socket. The sockets are generally known as 0, 1, and 2. COS (monitor program) occupies at least 4K of addressable ROM space and always occupies ROM in sockets 0 and 1 (COS 3.0, 3.4) or all three sockets (COS 3.0 [2708's in 1 and 2], COS 4.0 and COS 4.2 [2716's in 0, 1, and 2]).

Eleven address lines are required to uniquely address 2K of ROM. The least significant addresses BA0-BA10 are used to select the address within ROM to be read. Coarse address decoding is performed by PROMs M and P (ICs 13 and 19) using the most significant six bus address lines and one page bit. In this way, ROMn ENAB- is generated and each ROM is mapped into address space within a 64K page. Two pages are currently available: ROM 0 is mapped at 0000H on page 0 to execute code on power-up, and normal 380Z page 1 mapping is selected on setting the Page Sel bit in system port 0.

Once ROMn ENAB- is active (follows MRQ- timing) the 8-bit word stored at the specified address within the EPROM is transferred to the data output lines D0 -D7, and buffered onto the data bus by IC 11 (tristate uni-directional). IC 11 is enabled by the ANDed function of MEMRD- and ROMRD- (derived form ICs 17 and 19), which ensures that write operations to address space occupied by ROM does not cause a data bus crash. Space occupied by ROM is transparent to write operations.

Dynamic RAM and RAM Support

(Circuit 380Z : CPU/RAM)

There is space on the CPU board for up to 32K of dynamic RAM (4116 or similar) organised as two banks of 16K x 1 x 8 bits. Bank 0 must contain 16K x 1-bit RAM but provision is made both by hardware and software for bank 1 to be empty, or to accept 4K x 1 RAM, or to accept 16K x 1 RAM.

A complete diagram showing RAS and CAS timing within all memory cycles is

shown in figure 1.1. Measurements are taken when executing the following code:

```
0100            LD      HL,1000H
0103    LOOP:   LD      (HL),A
0104            JR      LOOP
```

Fourteen address lines are required to uniquely address each location within a 16K bank of RAM. Bus addresses BA0 to BA13 are applied to the inputs of two 2-1 multiplexers (ICs 5 and 6.) With the exception of a refresh cycle, BMRQ- is clocked on the first rising edge of the system clock, after MRQ- becomes active through D-type flip-flop IC 24, to a 'low' on output Q (pin 5). This output is used to switch the multiplexers between row and column addresses at outputs MA0 to MA7. CAS becomes active after a delay (IC 16 plus a 1000pF capacitor) allowing time for addresses to settle and for RAM to process the row address. RAS is generated by producing a coarse address decoded output of PROM M (IC 13) using BA14 to 16 and one page bit to map one bank of RAM to address space within a 64K page. This output selects the bank of RAM for a given 16-bit address and is NANDed with BMRQ- to produce RAS active from the falling edge of MRQ-. CAS is applied common to both banks of RAM. RAS is active during read/write cycles only to the bank being accessed. The precise address within a bank of RAM is selected by the multiplexed addresses MA0 to MA7.

LINKS L10-L12 adjust address multiplexing to provide outputs suitable for driving 4K x 1 RAM (4027, etc.)

Data input to the RAM is taken directly from the data bus. MEMWR- is active to instruct RAM to accept data during the memory cycle only during a RAM-write operation (IC 17).

Data output from the RAM is buffered by IC 2 and passed onto the data bus only when RAMRD- is active. RAMRD- is generated by producing a coarse address mapped output from PROM M (IC 13) which is ANDed with MREQ- and BRD-, to produce RAMRD-, only during read operations from RAM. RAMRD- timing should follow BMRQ- timing exactly during RAM read operations.

RAS-only refresh is maintained on all banks of RAM in the following way:

- CAS is inhibited by applying a 'high' on pin 2 of IC 17, thus ensuring that corruption of data does not occur during refresh.
- PROM M (IC 13) produces an output enabling RAS of both banks during the MRQ- signal active period (see figure 1.1).

System Clock

(Circuit 380Z : CPU-2)

IC 23 (4069) is used in a crystal-controlled 8MHz feedback-oscillator which produces a near-sinusoidal waveform on pin 10. Other segments of IC 23 are used to square the 8MHz clock; this is then taken to the VDU board (J2-9) and to IC 24 which is wired as a divide-by-two counter with output on pin 9

at 4MHz. This output is buffered onto the 50-way bus (J3-40) by IC 21, and also buffered by a different segment of IC 21 onto the processor. BCLK is the 4MHz system clock and is in phase with the 4MHz clock to the processor.

Memory-Mapped Port Decoding

(Circuit 380Z : CPU/RAM)

Coarse decoding circuitry is used to support memory-mapped ports, such as system port 0. The screen mapping is also coarsely decoded in this way. Using the more significant address lines and one page bit, PROMS 13 and 19 produce an output when the address bus contents correspond to either screen address or memory-mapped port addresses. Finer decoding of port addresses is carried out by IC 7, which gives an output IOSEL- when the address bus content is within the block of 4 port addresses. Both VDU SEL- and I/O SEL- are taken to the VDU board on the 37-way bus.

User Port Latches

A buffer (IC 3) and a latch (IC 4) on the CPU board, together with a 20-way connector, form the user port interface. Input/output is taken directly from the data bus, and control circuitry is found on the VDU board.

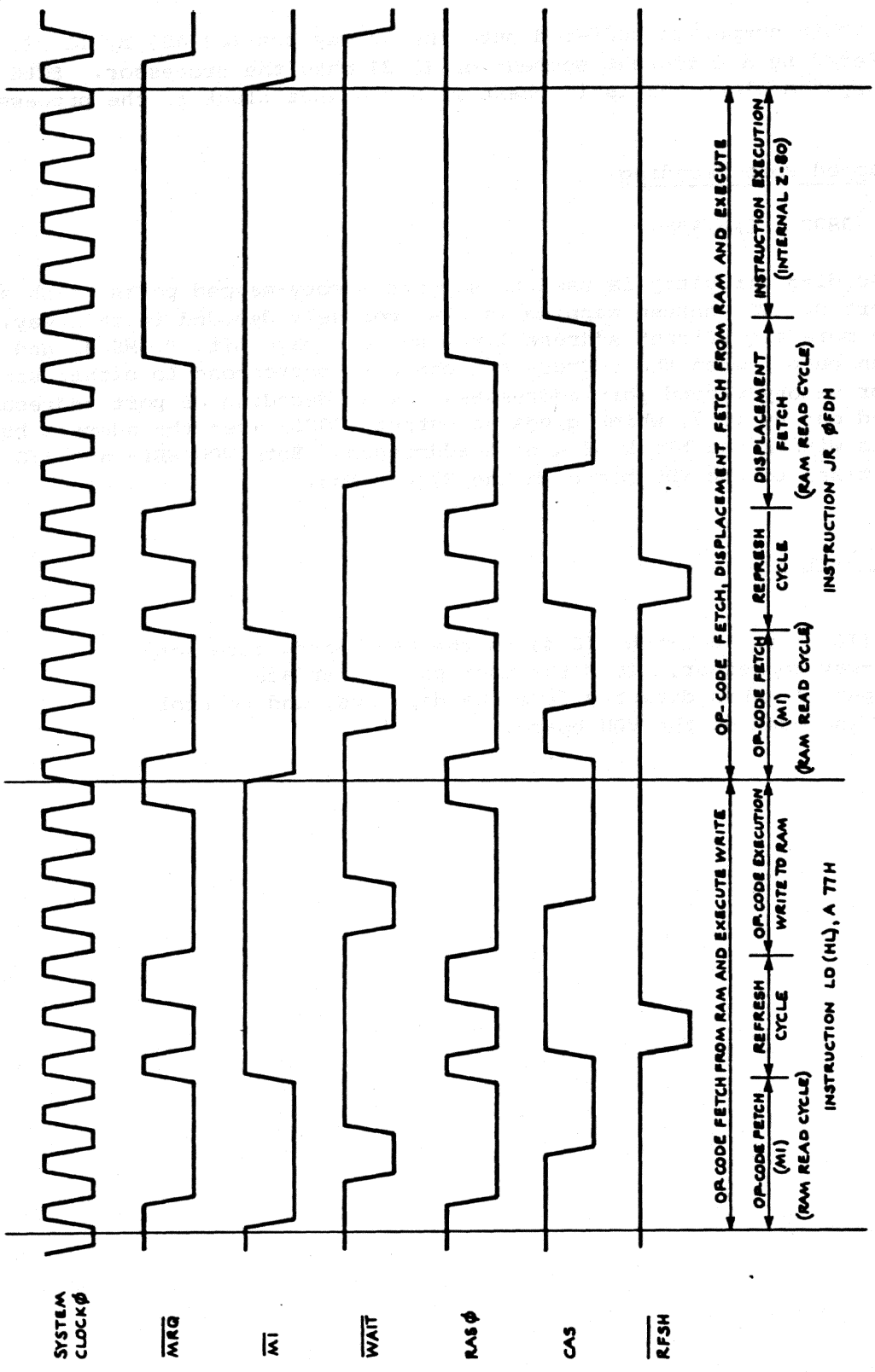


Figure 1.1 RAM Timing

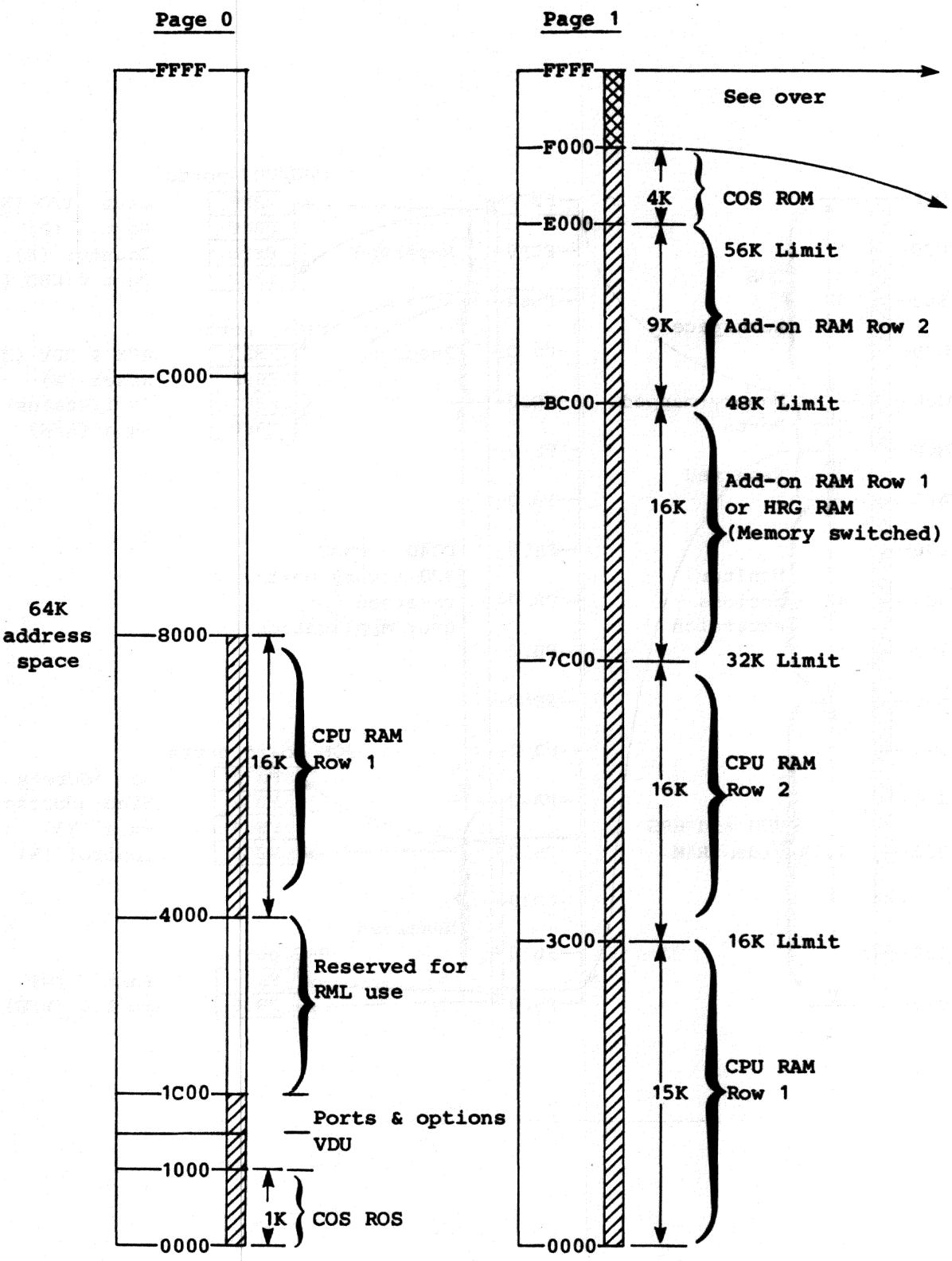


Figure 1.2 Standard 380Z Use of Memory

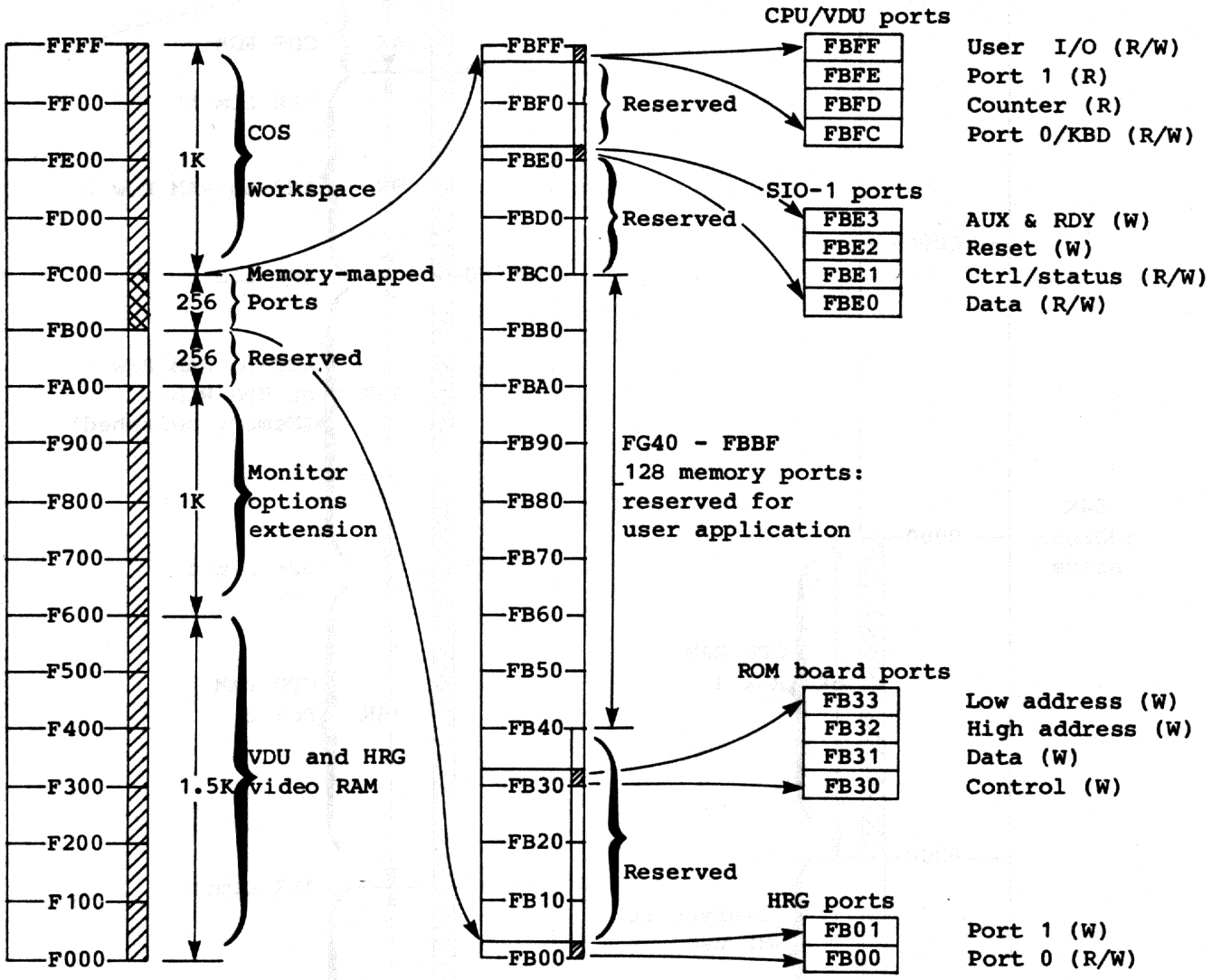
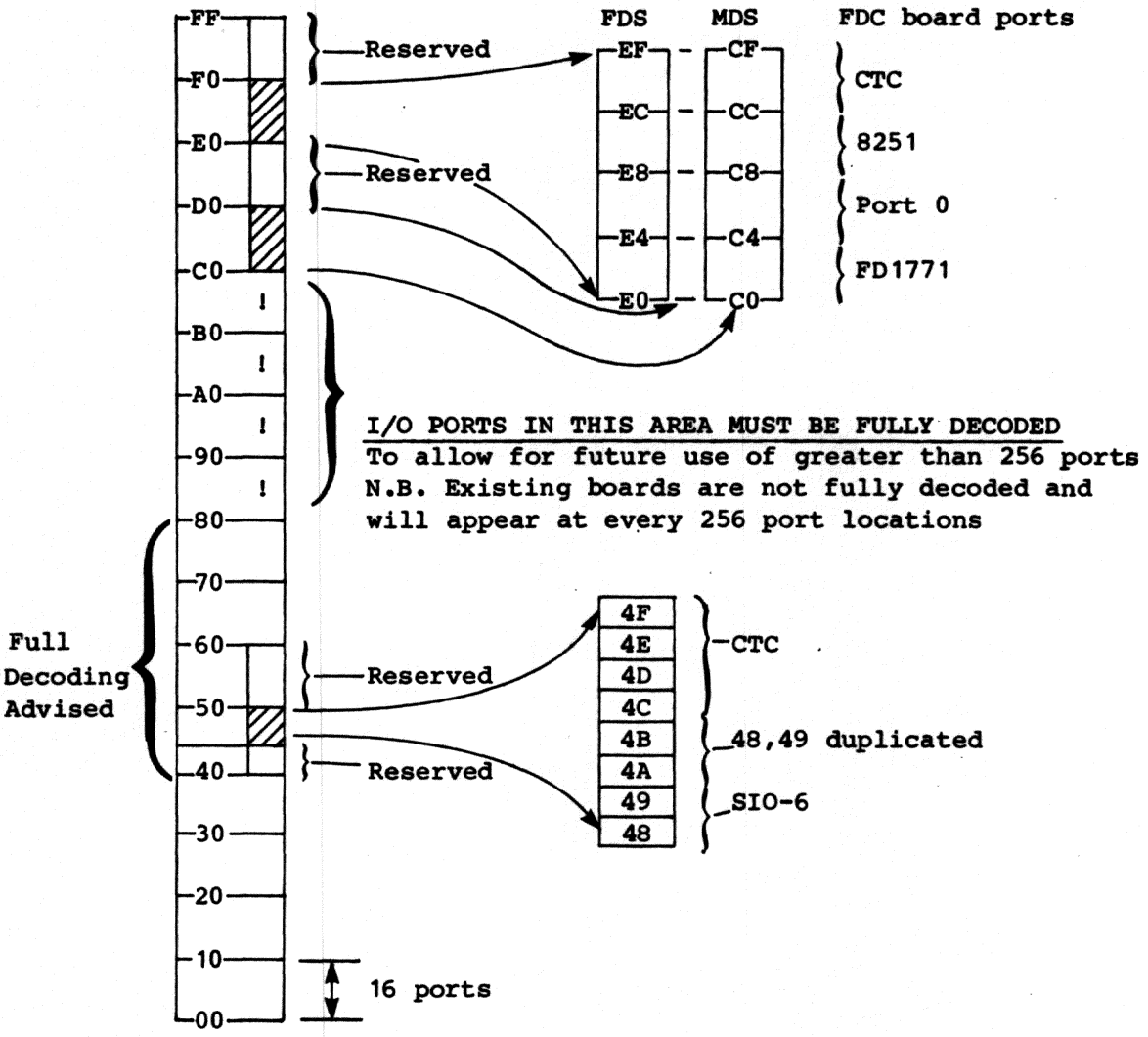
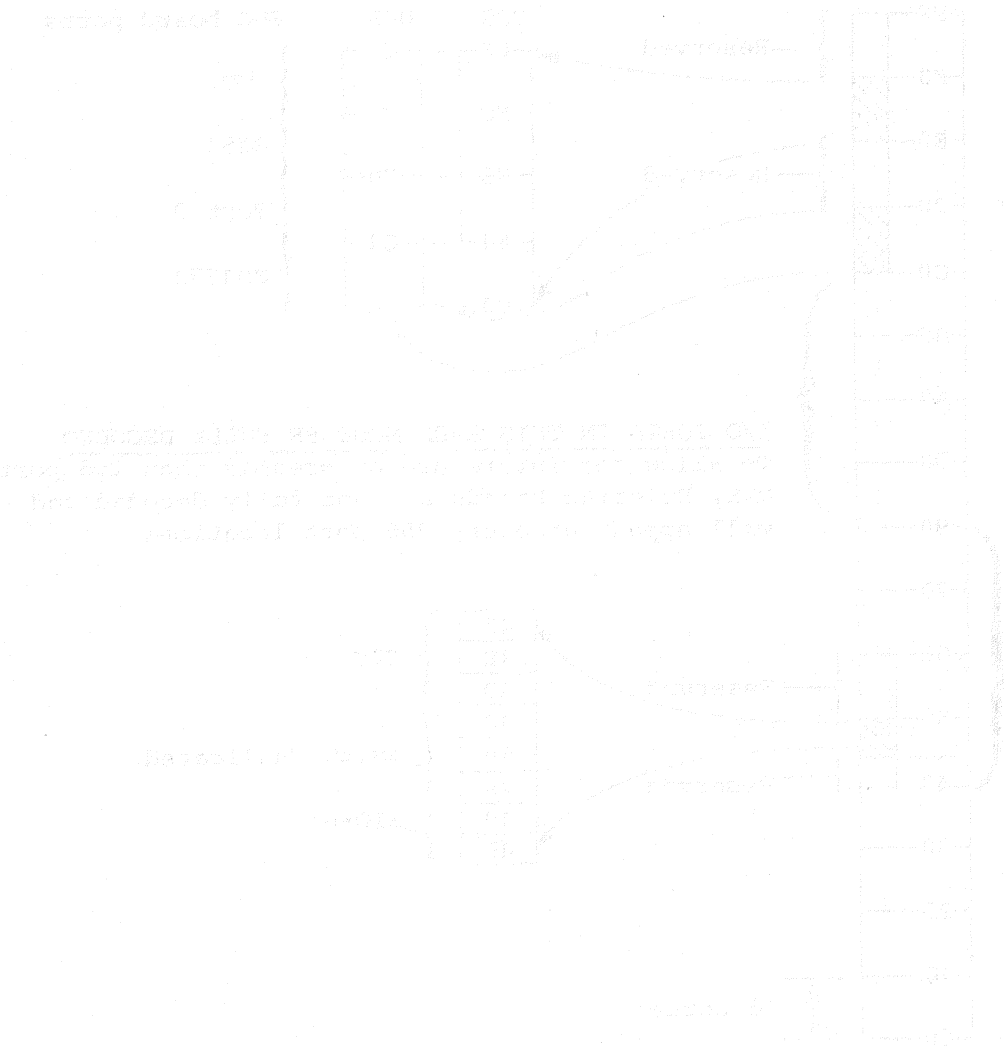


Figure 1.3 Page 1 Use of Memory Above F000



N.B. PIO boards occupy 16 consecutive I/O ports.
PIO + IEEE board occupies 32 consecutive I/O ports.
Users are advised to fill I/O ports from the bottom avoiding 40 to 5F if possible.

Figure 1.4 Standard 380Z I/O Map



SECTION 2

VDU-40 BOARD

INTRODUCTION

This section details the circuitry of the VDU board supporting CPU boards with COS versions 3.0 and 3.4. Early versions of the VDU board may have hardware modifications to the latest circuit specification. No attempt is made to document anything other than the current 40-character VDU board.

CIRCUIT DESCRIPTION

(Circuit Diagrams: 380Z : VDU-1, Keyboard and Cassette Interfaces, Ports and Video Memory.
380Z : VDU-2, Video Generation.)

The VDU board comprises:

- Screen generation hardware
- 1K of static screen memory
- Cassette-handling hardware
- CPU reset circuitry
- Keyboard port
- Three system ports
- User port control circuitry.

Screen Generation Hardware

(Circuit 380Z : VDU-2)

Both IC 30 (74LS393) and IC 33 (74LS73) comprise a 9-bit binary counter clocked at 8MHz from the CPU board. The 9-bit outputs are column counts CC0 to CC8. The column count is used to define a horizontal screen position. CC4-CC8 are used to count character positions along a screen line (row) and are fed into the line waveform generating PROM (IC 31, coloured green). The line PROM produces signals LINE ACCESS, LINE BLANKING, LINE SYNC., and a count output to clock the line counter. The signals are then latched by IC 34 on the rising edge of CC3. The LINE COUNT output clocks a 9-bit binary row counter (ICs 32 and 37) the outputs of which (RC0-RC8) define row positions within the screen. RC1 to RC8 are used by the FRAME PROM (coloured yellow) to produce signals FRAME RESET, FRAME BLANKING, FRAME SWITCH, and FRAME ACCESS.

The LINE and FRAME BLANKING signals are mixed by IC 25/1,2 to give a composite blanking signal on IC 25/3.

FRAME SWITCH is used by the line PROM to invert line sync pulses and double

their frequency during FRAME SYNC to maintain convention with television video sync signals.

LINE and FRAME ACCESS are available as bits in read port 1 and can be tested to open the Video RAM during line/frame blanking.

A 7-bit word read from the video RAM is decoded in the character generator IC 27 and identifies a unique character. The five outputs, Y1 to Y5, are the row dot pattern corresponding to the row within the character selected by inputs RC0 to RC3. Y1 to Y5 are latched by IC 28 at the start of each new row within a character, then fed to IC 29 (8-to-1 binary select demultiplexer); CC0 to CC2 select which of the five column bits to transfer to output pin 5 (IC 29). In this way, row data is shifted serially through IC 29 and becomes video information on pin 8 of IC 43 (if not inhibited by GRAPHICS- on pin 11, IC 43).

Video information is inhibited by composite blanking in IC 38, and VDU ON+ in IC 40. (VDU ON- is used to open the screen to write to the video RAM and is normally only active during screen blanking, to prevent flicker. VDU ON is under software control, and is a bit in system port 0). Video information, VIDG, is conditionally duplicated (condition = white graphics) to form VIDW. If VIDW is inhibited (grey-active) the video information formed by adding (analogue) VIDG & VIDW is half the amplitude that would be generated with VIDW active, and grey intensity results.

D1, D2, and R25 form the video/sync mixer. The video output stage is a common collector transistor impedance buffer. Output impedance is 75 Ohms and level 1V peak to peak composite video information, -ve sync. Power for the video output stage is derived from the 12V rail via R35 and D3. A simple UHF modulator accepts composite video input and produces a UHF modulated copy. Carrier channel is around channel 36.

The character generator (IC 27) is a TEXAS 74LS262 which has a teletext-compatible character set and is an industry standard. It accepts ASCII-coded input for codes in the range 0 to 128. Above these values, codes are interpreted by the VDU board as graphics characters. These are generated by the dual 4-to-1 binary select multiplexers, IC 35 and IC 42 (latch), from information encoded in the hardware of the logic array formed by ICs 38, 39, and 40. Graphics is selected from MD7 (ASCII codes greater than 128) and grey intensity is selected from MD6.

1K Static Screen Memory

(Circuit 380Z VDU-1)

One page of video information is stored in static RAM on the VDU board to enable screen displays of 40 x 24 characters. To uniquely address 40 characters in a line, six address lines are required, and, for 24 lines in a frame, 5 address lines are required. Thus, to specify each unique location on the screen as part of a rectangle would require 11 address lines. Using 1K static RAM, only 10 address lines are available, so it is necessary to address the screen as a 5x5 address square, and "move" part of the square to a screen position such that a 40x24 shape screen results.

The hardware of the VDU board automatically accommodates the transfer of screen address position by detecting when CC8 is valid and adjusting the output of multiplexer IC 14 accordingly. With the exception of this complication, multiplexers 11, 12, and 13 select between access to the screen for reading (row and column address specify character position) and access to the address bus for writing (a character written to a unique address corresponds to a character position when read back by the screen). Ten address lines, MA0-MA9, address the 1K of video RAM.

Data input is taken directly from the data bus, (BD0 to BD7), and is written to the RAM when VDUWR- is decoded by IC 25.

Data output from the RAM forms the bus MD0 to MD7 which feeds the character generator and graphic generator circuitry. Provision is made to read the video memory to the data bus, BD0 to BD7, by opening the screen (VDU ON- inactive) and transferring the MD bus to the BD bus via tristate buffer IC 26.

Cassette-Handling Hardware

(Circuit 380Z : VDU-1)

Binary counter IC 9 is clocked by a 16 us clock, CC6. It is wired as a divide-by-14 counter and the output is further divided by 2 and 4, yielding 2400Hz and 1200Hz on IC 9/10,11. These two clock frequencies are passed through active 'low' pass filters (IC 8) and appear as sinusoidal waveforms at the fundamental frequencies on IC 8/7,8.

The cassette recording format consists of selecting between cycles of 2400Hz and 1200Hz to encode serial information. The serial information to be encoded is generated under software control and appears as a bit in system port 0, SWITCH. SWITCH is converted to CMOS-compatible level via Q1 and drives the select input of a 2 - 1 analogue multiplexer (CMOS) IC 7. According to the level of SWITCH, either 2400Hz or 1200Hz is transferred through IC 7 and appears on IC 7/14 at a much reduced amplitude (approximately 100mV pk to pk) and via C1/R1 to connector J1-25 as CASSETTE OUT.

The cassette input is A.C., coupled via a low pass filter R3/R4/C2/C3 to a segment of op-amp IC 8 operated in open loop mode. Transitions between supply rails occur at the output pin 1 on each zero-potential transition on input pin 2. R11 converts the output level to be TTL compatible, and the signal produced is CASSETTE SIGNAL, which can be read as a bit in system port 2. Simultaneously, a bit is available in system port 2, CASSETTE VOLUME, which indicates adequate/inadequate signal strength on the cassette input line. Signal strength is detected by another segment of IC 8 wired as a simple comparator with a DC potential formed by R8 and R9. This amplitude detector is sensitive to phase and so the output can be used with CASSETTE SIGNAL to deduce the phase of the cassette input signal. All decoding of cassette data is carried out under software control by support routines within COS.

CPU Board Reset Circuitry

(Circuit 380Z : VDU-1)

- Power-on Reset:

  When power is first applied to the system, a small amount of dedicated circuitry ensures reliable system initialization and does not depend on CPU board signals being present (e.g. M1). A 4.7 uF capacitor is charged to +5V via a 33kohm resistor. Until the voltage upon the capacitor develops to a TTL logic 1, the SET and RESET inputs of the J-K flip-flop segments in IC 44 are held 'low', and 2400Hz pulses are transferred unconditionally to output pins 15 (Q- active high) and 14 (Q- active low). These outputs are SYSTEM RESET (transferred to CPU board) and Q- is used to reset system port 0.

- Manual Reset:

  Users can manually activate the system reset by means of the RESET button. When the RESET button is pressed, J-K flip-flop IC 44/12K input goes 'high'. With SET, RESET, J, and K inputs 'high', the outputs toggle with the 2400Hz clock input (generated in the cassette-handling hardware IC 9/11). The 2400Hz signal produced is clocked through the second segment of IC 44 on the falling edge of BM1-, ensuring that reset pulses only reach the Z80 during an op-code fetch and that the contents of RAM are not corrupted. There is sufficient time between reset pulses to maintain refresh to the dynamic RAM in the system. System port 0 latch IC 1 is reset simultaneously with system reset.

System Ports, Keyboard Port, and User Port Decoding

(Circuit 380Z : VDU-1)

Coarse port decoding is carried out on the CPU board and the 4 ports are mapped to occupy the following positions within the memory map:

	PORT 0	PORT 1	PORT 2	PORT 3
PAGE 0	1BFCH	1BFDH	1BFEH	1BFFH
PAGE 1	FBFCH	FBFDH	FBFEH	FBFFH

Port 0 Read:keyboard port Write:system port 0

PORT 0 BIT ALLOCATION:

READ	BIT	WRITE
KBD BIT 7	7	PAGE SELECT (0=PAGE 0)
KBD BIT 6	6	CLR COUNTER (1=CLEAR)
KBD BIT 5	5	CTRL 2 (Cass. motor)

(Cont'd)

KBD BIT 3	3	CTRL 1 (Cass. motor)
KBD BIT 2	2	VDU ON- (1=Screen Open)
KBD BIT 1	1	NMIEN- (0=NIM enabled)
KBD BIT 0	0	KBD CLR+

Port 1 Read:counter Write:no port

PORT 1 BIT ALLOCATION:

READ	BIT	WRITE
62.5 kHz	0	-
31.25 kHz	1	-
15.625 kHz	2	-
7.81 kHz	3	-
3.91 kHz	4	-
1.95 kHz	5	-
975 Hz	6	-
487 Hz	7	-

Port 2 Read:system port 2 Write:no port

PORT 2 BIT ALLOCATION

READ	BIT	WRITE
LINE ACCESS	7	-
FRAME ACCESS	6	-
CASSETTE SIGNAL	5	-
-	4	-
CASSETTE VOLUME	3	-
RESET BUTTON	2	-
1200Hz	1	-
KBD STROBE	0	-

Port 3 Read:user port Write:user port

IC 23 is used to uniquely decode each of the 4 ports using IOSEL- from the CPU board and BA0, BA1, MEMRD-, and MEMWR-.

The keyboard port functions as follows: A negative-going edge of a keyboard strobe clocks data into two 4-bit latches which form read port 0. KBD STROBE is also available as a bit in system port 2 (read port 2) and is tested to detect keyboard input. Keyboard data may then be read from port 0; the latches may be cleared by setting bit 0 in system port 0.

SECTION 3

VDU-80 BOARD

INTRODUCTION

This section details the circuitry of the 80-character VDU (VDU-80) board supported by COS 4.0. The board operates in two modes:

1. 24 lines by 80 characters

2. 24 lines by 40 characters

The circuit is complicated in mode 2 by the need to maintain hardware compatibility with the existing 40-character board.

CIRCUIT DESCRIPTION

(Circuits :	VDU 80-1	80/40	VDU	TIMING/PORTS
	VDU 80-2	80/40	VDU	MEMORY
	VDU 80-3	80/40	VDU	BUS BUFFERS
	VDU 80-4	80/40	VDU	OUTPUT)

Timing

(Circuits VDU 80-1, VDU 80-3)

The 80-character display requires a dot rate of 16MHz. However, to operate correctly in conjunction with the HRG board, the 16MHz must be synchronized with the system clock. It is derived from the 8MHz available at the 34-way connector. This signal is almost sinusoidal and is squared by IC CP (74L221). The two outputs of this monostable drive IC DP (74221) which produces pulses on both rising and falling edges. These are combined by EP (74LS02) to give the signal C16M. In 80-character mode, this signal should be at 16MHz with a 1:1 mark space ratio. In 40-character mode, alternate pulses should be missing.

The character rate, CRATE-, is generated by counter GP (74LS169A or 74LS168A or equivalent, but not 74LS668 or 74LS669), which counts down from 7 to 0 during each character. CRATE- indicates that the last dot of a character is being displayed and is used to enable the loading of various registers.

The main dividers GU (74LS393), FT (74LS390) and FV (74LS393) are similar to the standard 40-character VDU board. Their outputs drive PROMs FU, EU (74LS287 or equivalent) which generate blanking and synchronization signals. Separate vertical and horizontal syncs (VDRIVE and HDRIVE) are available for a "wire frame" type monitor. Note that all the PROMs have

4K7 SIP pull-ups on their outputs to allow use of open collector types without needing the "piggy-back" resistor network.

Hardware Scroll

(Circuit VDU 80-1)

Hardware scroll is performed by adding a number to the output of the row counter, modulo 24. This has the effect of scrolling the display by that number of lines. The number to be added is in the low 5 bits of CR (74LS377). This is memory mapped at FBFD. However, the port can only be written to when the screen is closed, so it cannot be done directly from the Front Panel. The addition is performed by ES (74LS283) and FR (74LS287).

Address Multiplexers

(Circuit VDU 80-1)

The VDU can be written to "transparently". That is, it is not necessary to wait until line or frame blanking takes place. This is achieved by cycling the memories twice per character, once to get the character and once for the CPU. The CPU and VDU addresses are multiplexed by AR (74LS157), CT (74LS257) and AT (74LS399). CS (74LS399) performs the translation from 32x32 to 24x40 as on the 40-character VDU board. The multiplexers CS and AT contain a latch on their outputs clocked twice per character. The remaining address lines are latched by DT (74LS175). When in 80-character mode, four address bits are latched in DU (74LS173).

Character and Attribute Memory

(Circuit VDU 80-2, VDU 80-3)

The characters are stored in CW (HM6116) while the attribute bits are held in BU and CU (2114). The characters are latched in DW (74LS273), and the attribute bits in part of AS (74LS374). The characters are read and written using DV (74LS245). When a character is written, the corresponding attributes are cleared. For this purpose, 1k2 pull-ups are provided on the data lines of EU and CU. When the attributes are themselves to be read or written, the data is passed through DR (74LS240).

The data bus buffers consist of BR (74LS373) and AQ (74LS244). BR is a latch to hold the data long enough for a write to take place when using the 'transparent' mode.

Character Generator

(Circuits VDU 80-1, VDU 80-2)

The character generator is the ROM EW (2516 or 2532) together with the RAM GW (HM6116P). The information from the character latch is applied as an address to these memories along with four bits from the row counters. The data is latched in the shift register GV (74LS166) from where it is shifted out as video information. The RAM portion of the character generator

allows for user-definable characters. To store these characters, both address (to select one row of the character) and data (the dot pattern for that row) must be supplied. The character generator can also be read back by the CPU.

Data is applied through EV (74LS245); the address is more tricky. The high eight bits must be latched in DW (74LS273) via DV (74LS245) by writing to a port at FBFE with bit 3 (CGSEL) of the control port at FBFC set. The remaining four bits are written to the latch DU (74LS173) which is also mapped at FBFE but which is only available when the screen is closed. (Note: The outputs of this latch are connected to the same lines as the outputs of the multiplexer CT (74LS257). This is because the same latch, DU, is used to supply some of the address bits to the character store when accessing the screen in 80-character mode.) The multiplexer ET (74LS399), which includes a latch, selects either the row counters (normal display) or DU (writing to character generator, or during a smooth scroll) as the source of the four low-character generator address lines.

Control

Control signals from the CPU are buffered by AP (74LS244). Whenever possible, signals are taken from the bus connector rather than from the 34-way connector. The bus buffer direction is controlled by logic contained in CQ (74LS27), DR (74LS02), and FP (74LS266).

BS (74LS155) is a decoder for the ports at FBFC to FBFF. The signals PORT3 WR- and PORT3 RD are sent back to the CPU to enable the user I/O port. The latches ER (74LS273) and CR (74LS377) supply miscellaneous control bits as shown on the diagrams. Half of AP (74LS244) is used to monitor KBDSTB,VBLANK and HCPUEN.

Keyboard

(Circuit VDU 80-1)

The keyboard port is CV (74LS374). As this cannot be cleared, a separate latch made from two gates in FQ (74LS132) is provided to catch the strobe. A filter (R11 and C5) is provided on the strobe line. One section of the Schmitt-trigger EQ (74LS240) is used to clean up the signal which is then differentiated by R9, R10 and C6 to provide a short pulse to set the latch. This allows the use of a keyboard which produces a level while a key is held, as opposed to a short strobe.

Reset

The reset circuit is similar to the current one (as VDU40)

Character Write Signal

The generation of the write strobe to the character store is complicated by the transparent access. When the CPU performs a write operation, it must be delayed until the memory has finished the current character access. One section of FT (74LS390) is used simply as a flip-flop to remember that a "write request" has occurred. This is synchronized to the VDU timing by

the latch DY (74LS374) and from the latched signal a write strobe is generated by the monostable BP (74221). This strobe also clears the latch FT.

CTC

The CTC allows interrupts to be generated from the keyboard strobe, from the vertical blanking signal, or from the line frequency. The only non-standard thing here is the address decoding. To avoid a separate decoder, it is mapped in I/O space at FBFC to FBFF, i.e. register B must contain 0FBH, when writing or reading the CTC with an OUT (C), A or IN (C), A instruction.

Video output

The output stage has to deal with twice the bandwidth as compared to the 40-character VDU board. It must provide outputs for "wire frame" monitor and combine the output from the HRG board with that from the VDU. Further, it has to process the information contained in the attribute memory.

Inverse video is achieved using the XNOR gate FP (74LS266). This is an open collector gate and the blanking signal is introduced at this point. Dim video works as on the 40-character board. Two currents are added in the output stage in a crude D to A converter.

Underlining is performed by modifying an address line to the character generator with gates from GQ (74LS09) and GS (74LS32) so as to display a portion, not normally visible, which contains the underline.

In the output stage itself, T1 is a common base stage to amplify the HRG signal, with T2 after it as an 'emitter follower'. The open collector driver BV (7407) buffers the video signals which are added in the resistor network R18, R19, R20, and R23, along with diodes D3, D4, and D5.

Diodes D2 and D6 introduce the sync signal. D7 is a level shifter to ensure that sync goes down to zero. T3 is a final emitter-follower stage. T4 is used to disable the video signal from and to the HRG board.

Smooth Scroll

This uses hardware which has already been described.

During normal display, the multiplexer ET (74LS399) takes the dot row number from the first stage of the vertical counter FT (74LS390). When the smooth scroll is being performed, this multiplexer is switched over to take the dot row number from the latch DU (74LS173). Thus the CPU controls the rows to be displayed. In conjunction with the scroll count in CR (74LS377), the software can make the picture move by one row of dots per frame, giving the appearance of a smooth scroll.

SECTION 4

FLOPPY DISC CONTROLLER BOARD

INTRODUCTION

This section details the circuit description of the floppy disc controller board (FDC) used in all 380Z disc systems. Hardware differences between versions, for supporting different drive types, are included.

CIRCUIT DESCRIPTION

(Circuits : 380Z Floppy disc controller and SIO4, FDC1 and FDC2.)

The floppy disc controller board contains circuitry of two types:

1. Hardware to support a serial interface with full handshake - the SIO4 port.

2. Circuitry for dedicated disc-controlling purposes.

The board is accessed as a block of ports in I/O space, mapped as follows:

FDS	MDS	SIO6	FDS Board Ports
=======EF	=========CF	=========4F	========
=======EC	=========CC	=========4C	======== CTC
=======E8	=========C8	=========48	======== 8251
=======E4	=========C4	==========	======== PORT 0
=======E0	=========C0	==========	======== FDD 1771

1. Bus Buffering and Port Decoding

(Circuit : FDC1)

The least significant eight bus address lines BA0 to BA7 are buffered by IC AQ and become IA0 to IA7. The board is accessed using I/O instructions such as OUT (C),A...IN (C),A etc. The port address appears on the least significant eight address bits. IC BQ and BR (3 to 8-line

binary select line decoder) decode IA2 to IA7 to establish the map in I/O space (as above). IC BR has four outputs, CTC EN-, 8251 EN-, 1771EN-, and port 0 enable. Each of these represents a block of four ports corresponding to each function. All four outputs are ORed by IC BQ to produce IOEN-. Links 10 and 12 select whether the board is to be mapped as a full (links cut) or mini (links present) system disc-controller board.

Data is transferred via the bi-directional tristate buffer, IC AR. The direction of transfer is selected by the logic array formed from ICs CP and BP. This uses either IOEN- and IRD- to detect when one of the ports on the board is to be read by the CPU, or INT- at the first IM1- low, with IIORQ-, to reverse the direction of the buffer. IC BP /9 ensures that the direction is reversed only during IORQ operations.

Bus and CPU control signals are buffered by IC AP. On the circuit diagram these signals have the prefix I.

Port 0 is not fully decoded and occupies all four port addresses within the block assigned to it. IC BP/6,3 produces IORD- and IOWR- from IIORQ-, IRD-, and IWR-. IOWR- is active during all I/O writes within the system, and is used by IC BP/11 to enable the port 0 latch, IC BS, only during I/O writes to port 0.

Port 0

(Circuit : FDC1)

Port 0 consists of an 8-bit latch, IC BS, into which the contents of the ID bus may be written. It is a write-only port and cannot be read back, so a mask is held in memory of the contents. All software access to the port must be via read-modified write sequences.

Port 0 Bit Allocations:

Read	Bit	Write
-	7	DINT- (Force disc interrupt)
-	6	SET DRIVE EN-
-	5	MSEL (Dir/side select bit)
-	4	SSEL (Side select bit)
-	3	DS4 (Motor on)
-	2	DS3 (Drive select bit 2)
-	1	DS2 (Drive select bit 1)
-	0	DS1 (Drive select bit 0)

CTC Usage

(Circuit : FDC1)

IC DQ on the FDC board is a Z80A CTC. It is fully supported and is used extensively for both disc control and SIO4 implementation. It occupies a block of 4 channels, each of which is uniquely decoded by IA0 and IA1 in

I/O space. For all normal applications used by the monitor, interrupt requests are not generated although provision exists for future expansion.

Channel 1: Drive enable timer. Used for drive software timings

Clock input: 64ms with DRIVE ENABLE-

Channel 2: Head load timing register. Used for drive software timings.

Clock input: 2ms with HLT and HLD

Channel 3: Clock generator for UART Baud rate (SIO4)

Clock input: 2MHz

Channel 4: Clock input: 64ms

For disc control applications the CTC is used under software control by disc I/O routines in the monitor to generate disc primitive timings, i.e. DRIVE ENABLE, HLD delay etc. Flip-flop IC ES is used extensively to implement the timing of these signals. The CTC is clocked from the system 4 MHz buffered clock, ICLK2.

8251 Usage SIO4 (SIO6)

(Circuit : FDC1)

To implement a full V24 RS232 serial port, a dedicated UART IC, ER (8251), is used. This makes for very simple operation. Access to and from the UART by the CPU is through the block of ports occupied in I/O space. Input/Output from the UART to the serial port is via RS232 level drivers/receivers, ICs AV and BV. Control of data exchange in the port is under software control by the CPU, and baud rate for transfer is controlled by the rate of the TXC and RXC clock inputs. These are commonly derived from the CTC channel 2 after monostable IC DU produces active 'low' clock pulses of duration 1.5 us (approximately). Connection to the external peripheral is via J1.

2. Dedicated Disc Controller Circuitry

(Circuit : FDC2)

Disc I/O is largely handled by a dedicated IC controller, the FDD 1771, which occupies IC position CS. Access to the controller is via the block of ports which it occupies in the I/O map. Disc control outputs are buffered by open collector driver ICs AS and AT. Inputs are pulled up via 150 Ohm resistors to +5V, then buffered by IC AU. Links are clearly marked on the circuit diagram where hardware differences between full and mini-disc systems exist.

Apart from the FDD 1771 and support, a DATA/CLOCK separator circuit is included. This separates interleaved 'data' and 'clock' pulses from the disc drive READ DATA input into the FDD and FDC inputs to the 1771. It operates in the following way: an active 'high' clock pulse (FDC) is inverted (IC ET/8) and loads a 4-bit binary counter (CT) with 12. The counter counts up with a clock period of 250ns (full system) or 500ns (mini system) and places its count output in a BCD to decimal decoder (DT). When the count is zero, the zero output of DT goes 'low' and is used to set an S-R flip-flop (ET) whose outputs are DATA WINDOW and NOT DATA WINDOW. ET is reset when the binary count reaches 7 and DATA WINDOW is inverted until the next clock pulse, and the cycle is repeated.

Data and clock pulses (interleaved) are taken from the disc drive and passed through a Schmitt-trigger buffer, then through a monostable of time constant 120ns (approximately), before being ANDed (EU) with DATA WINDOW and NOT DATA WINDOW. The resulting outputs are separated 'data' and 'clock' pulses, FDD and FDC. (CU is used to set the phase of DATA WINDOW using the sector header before the sector identifier).

IC BT is used to multiplex direction and side-select information according to MSEL in port 0. Direction is decoded on the drive to be active with STEP, otherwise side-select information is assumed.

SECTION 5

INTELLIGENT DISC CONTROLLER BOARD

INTRODUCTION

This section describes the low-level hardware operation of the intelligent double-density disc controller board (IDC). The overall design objectives are first examined, followed by the general method by which each individual block or module is used. Then the detailed working of each module is considered in some depth.

Finally, the on-board firmware together with the option ROM interface is covered with the same top-down approach.

DESIGN OBJECTIVES

The IDC board was conceived as an improvement over the present disc controller board (FDC) in terms of storage per disc, speed and ease of use. The storage capacity has been increased by using double-density MFM recording and also by allowing for the use of 96 TPI mini-drives. Due to the use of MFM data recording the data is read from the rotating disc at twice the rate previously managed, and also, due to the use of on-board data buffering, the data throughput has been increased considerably in most uses.

As the board is intended to replace the present FDC, a serial channel is included with the same connections to the outside world. As a more modern serial chip has been used on the IDC than on the FDC, there are, in fact, two independent serial channels.

Another objective is that the board should be capable of working with a LINK 480Z. This has been made possible by allowing communication with the host processor (380Z or 480Z) through either the parallel (Z50) bus or one of the serial channels.

As the board is required to work with frequent interrupts, such as in a network server, it should carry out it tasks autonomously and without failing if interrupted during a data transfer. This is achieved by having an on-board Z80A microprocessor to handle the sectors coming from, or going to, the disc in real-time, and by transmitting the data between the host processor and the IDC under software control.

THE HARDWARE

(Circuits:

380Z Bus Interface and Decode:	DC 1/4
Disc Drive Interface:	DC 4/4
CPU, Serial Interface & Clocks:	DC 2/4
Memory, Wait State and Internal Decode:	DC 3/4)

The circuit consists of several clear-cut modules together with a small amount of TTL 'glue' to interface the various modules with each other. The main modules are as follows:

- Bus Buffering: to connect the board to the 380Z Z50 bus.
- Bus Interface: the method of transfer of data and commands to the 380Z. This includes two sub-modules:
  1. Data and status registers.
  2. Wait-state generation and time-out protection.
- External Decoding: to decode the I/O ports used by the 380Z.
- Clock Generation: to generate all clocks for the system including those for the serial interface, CPU and disc controller.
- Serial Interface: two channels of RS232 with buffering.
- Memory: on-board RAM and EPROM.
- Internal Decoding: to decode the I/O ports and memory used by the Z80A on the IDC board.
- Control Ports: to hold static values which control the disc drives.
- Disc Control: which consists of two sub-modules:
  1. FDC chip and buffers.
  2. Data Separator.

These various modules will now be described in more detail.

Bus Buffering

This consists mainly of three 74ALS1244N uni-directional buffer chips (IC 5, IC 10 and IC 11) to receive the addresses, and one 74ALS1245 bi-directional buffer chip (IC 4) which is used for the data transfer channel. In addition to these there is one element of an open-collector inverter (IC 3) which drives the WAIT line on the bus, and a three-input AND gate (IC 29) for the interrupt-priority daisy chain. The interrupt signal INT- from the CTC is also buffered by one segment of IC 1/4 to produce the BINT- signal.

Both the uni- and bi-directional buffers are permanently enabled with the direction control on the bi-directional buffers being driven by a BDIR- signal from a PAL (Programmable Array Logic) 12L6 (IC 19). BDIR- is 'low' when (i) the 380Z is reading anything on the IDC and (ii) the IDC is in the process of an 'interrupt acknowledge'. Otherwise BDIR- is 'high'.

The addresses and control lines can be connected to the bus of the IDC processor instead of the host 380Z, so that the 480Z version of the board will have access to the externally mapped ports; notably the CTC and SIO.

Bus Interface

(Circuit: DC 1/4)

1. Data and status ports are implemented as follows:

   There are two data ports made up of two octal latches, IC 9 and IC 18 (both SN74ALS574N). One supplies data to the internal Z80 and the other supplies data to the host Z80 bus. Both are edge-triggered 'D' type flip-flops with tristate outputs. Given the correct conditions, the host Z80 writes to the IDC data port on the low-to-high transition of the signal HWR-; this signal is, in turn, enabled by signal DRD- and so data is transferred to the internal Z80. Similarly, when the internal Z80 wants to transfer data to the host Z80, data is latched on the low-to-high transition of DWR- and is read by HRD-.

   It is important that communications between processors are kept in order to ensure that both processors do not try to:

   (i) read or transfer data at the same time
   (ii) transfer data before existing data has been read
   or (iii) read non-existent data.

   This is achieved by setting a status bit whenever data is written to a port. This prevents any further writing until the current data has been read by the alternate processor. If a further write is attempted, or a processor tries to read unwritten data, a 'wait' state is generated.

2. The 'wait' state generated by attempting to read non-present data (or to write to a non-cleared data port) is set and cleared by the positive edge of the relevant cycle. As flip-flops with an edge-triggered SET and an edge-triggered CLEAR are unavailable, this function has been built using the 74LS74 clock input to set the state, and an edge-detection mechanism to clear the state. The edge-detection is done on the write signal (HWR-, DWR-) by delaying and inverting the signal (to give DHWR and DDWR), then ANDing the two signals. This produces a CLEAR pulse of 125ns (less various propagation delays.)

   There are two flip-flops (IC 20 A and B), one to represent the state of the data bus interface in each direction. Flip-flop 'A' is CLEAR

(HWRWT- is 'low', DRDWT- is 'high') when data is available to the internal Z80A and thus cannot be written to again by the host Z80A. Flip-flop 'B' is CLEAR (DWRWT- is 'low', HRDWT- is 'high') when data is available to the host Z80A and thus cannot be written to again by the internal Z80A.

Take the flip-flop 'A' as the example: when the host Z80A writes to the data port, the flip-flop is set CLEAR at the end of the write cycle by the edge-detection mechanism. When the internal Z80A comes to read the data port, the flip-flop is SET at the end of the read cycle using the 74LS74 edge-triggered clock input. If the host Z80A tries to write to the data port whilst the flip-flop is CLEAR (or tries to read the data port when flip-flop 'B' is set) then a 'wait' state is generated and a time-out is initiated by triggering a 74LS123 (IC 30).

If the 'wait' state persists for longer then 200us or so, a fault has occurred; the 74LS123 will terminate and cut-off the 'wait' state to the host Z80A. It is conceivable that the software could recover from this situation in some circumstances, so a flag is set (DTIMED or HTIMED) if this time-out occurs. Also, to speed up any INIR or OTIR that may be in progress at this point, further 'wait' states are disabled until the status port has been read by the host Z80A. This latter function is accomplished using a 74LS107 as the time-out flag. The 74LS107 also holds off superfluous 'wait' states by grabbing hold of the CLEAR line on the 74LS123.

The 'wait' state and time-out structure for both directions is similar except for the actual time delay used. It is possible that the host system may be interrupted (e.g. if multi-tasking) and will leave the IDC board alone for quite a while. Therefore it is desirable to have a long time-out period for the IDC board and avoid the need for dynamic RAMs. Since the initial IDC design there has been a great improvement in communications software. Consequently, 'wait' states and 'time-outs' are avoided, especially on standalone 380Z-D systems where HRG RAM could easily be corrupted.

External Decoding

(Circuit: DC 1/4)

The bus direction signal BDIR- is decoded by six address lines, IA2 to IA7, together with control signals IIORQ, IWR and IRD. This is done to:

(i) enable the CTC and SIO (CTCEN- and SIOEN-)
(ii) read the host Z80A status port (HSTRD-)
(iii) read the internal Z80A data port (HRD-)
and (iv) write to the host Z80A data port (HWR-).

The PAL decodes I/O ports as follows:

CTC E0H to E3H

E0: CTC channel 0 (SIO channel B Rx/Tx clock) - read/write
E1: CTC channel 1 (SIO channel A Tx clock) - read/write
E2: CTC channel 2 (SIO channel A Rx clock) - read/write
E3: CTC channel 3 (completion interrupt) - read/write

SIO E4H to E7H

E4: SIO channel A data - read/write
E5: SIO channel A control - read/write
E6: SIO channel B data - read/write
E7: SIO channel B control - read/write

I/F Status E8H to EBH

E8: IDC interface status (Port 2) - read only
E8. IDC reset - write only
E9: IDC reset - write only
EA: IDC reset - write only
EB: IDC reset - write only

I/F Data ECH to EFH

EC: IDC interface data/commands (Port 1) - read/write
ED: IDC interface data/commands (Port 1) - read/write
EE: IDC interface data/commands (Port 1) - read/write
EF: IDC interface data/commands (Port 1) - read/write

If the host tries to write to the interface status port, both the signals HWR- and HSTRD- are generated, which cause the IDC board to be reset.

Clock Generation

(Circuit: DC 2/4)

The clocks generated on the board fall into three classes:

- Standard drive clocks of 1MHz, 2MHz and 4MHz
- A special drive clock of 4MHz
- "Times 16" baud-rate clocks with programmable frequencies.

A basic 8MHz crystal oscillator (XTAL, IC 45) is used to generate the initial timing. This signal is then buffered and passed to a divide-by-2, then 4, then 8 counter (half of a 74LS393 (IC 28)) to generate the standard 4MHz, 2MHz and 1MHz clocks respectively.

The 4MHz signal is passed through an invertor (IC 45/9) with a 330 Ohm pull-up to generate the CPU clock, PHI.

The 2 MHz signal is used as the trigger input for channels 1, 2 and 3 of the CTC (IC 44) which can be programmed to generate the desired "times 16"

clocks for the serial channel 'A' transmit and receive, and also for the serial channel 'B'.

Serial Interface

(Circuit: DC 2/4)

The serial interface consists of an SIO chip (IC 40) using 75188 line drivers (IC 15, and IC 16), and 75189 line receivers (IC 6, and IC 7). The signal levels on the lines are nominally +12V and -12V. The channel 'A' is selectable to use the Sync pin as Ring Indicate whilst the channel 'B' Sync pin is used for Data Set Ready. All the incoming serial control lines have 4K7 pull-up resistors to enable sensible use of the interface without the use of the handshake lines. The channel 'A' times 16 clocks are also jumper selectable to come from an external pin multiplexed with the Ring Indicate.

Memory

(Circuit: DC 3/4)

There are two sockets on the board capable of taking memory devices. One is for EPROMs (IC 47) and one for RAMs (IC 43).

The internal firmware ROM can take any sort of 5V-only EPROM, up to 8K by 8, by means of a set of links. These links are preset to take Intel-type 2764 EPROMs. The links for other devices, are as follows:

EPROM	LINKS	
2516/2716	3-5, 8-10	
2532	3-5, 6-8	
2732	5-6, 8-10	
2564	2-4, 5-7, 6-8, 9-10	
2764	3-4, 5-6, 7-9, 8-10	(this is the default option)
68764	5-7, 6-8	

The internal workspace and sector buffer RAM can be either a 2K by 8 or 8K by 8 RAM. The links required for these are as follows:

2K by 8	1-2
8K by 8	2-3

Internal Decoding

(Circuit: DC 3/4)

The decoding for all the chips accessible by the internal Z80A (IC 46, circuit DC 2/4) is done in a 10 input, 8 output PAL (IC 46, PAL 10L8) using address lines 2, 3, 7, 13, 14, and 15 together with control lines RD-, WR-, MREQ-, and IORQ-. The PAL decodes I/O-mapped port signals FDCEN-, DSTRD-, DRD-, DWR- and CTLWR- as well as memory-mapped signals ROMEN- and RAMEN-. There are two internal control ports which are enabled by address lines A0

and A1. The decoding is incomplete and, therefore, many different codes can access the same hardware. The nominal memory and port addresses are as follows:

FDC Chip 00H to 03H

00: Status Register	- read only
00: Command Register	- write only
01: Track Register	- read/write
02: Sector Register	- read/write
03: Data	- read/write

I/F Status 04H to 07H

04: Interface Status	- read only
05: Interface Status	- read only
06: Interface Status	- read only
07: Interface Status	- read only

I/F Data 08H to 0BH

08: Interface Data/Commands	- read/write
09: Interface Data/Commands	- read/write
0A: Interface Data/Commands	- read/write
0B: Interface Data/Commands	- read/write

Port 0 0EH
Port 1 0DH

Buffer RAM E000H to FFFFH
Internal ROM 0000H to 1FFFH

If the ROM is enabled, one 'wait' state is generated using half of a 74LS109 (IC 23) which is cleared at the end of the cycle.

Control Ports

(Circuit: DC 3/4)

The two ports used to control the static functions of the disc drives, such as side and drive select, are edge-triggered registers. They are written with a pulse (CTLWR-) from the internal decoding PAL (IC 42) and enabled with two separate address lines.

Port 0 (IC 39, SN74LS377N) contains the signals for drive selects, side, motor monostable trigger (IC 21, SN74LS377N) and confidence LED driving. The motor signal to the drives is SET by changing the motor bit from a zero to a one. The confidence LED is switched on if bit 6 is 'high' and bit 7 is 'low'.

Port 1 (IC 34, SN74LS379N) contains both the true and the false signals for drive size, bit density, and write pre-compensation enabling, and a flag for 'IDC in use'.

Disc Control

(Circuit: DC 4/4)

1. All output signals to the disc drives are driven by open-collector chips (IC 1, IC 3, and IC 8) and input signals are received by Schmitt-trigger buffers (IC 2) with 150 Ohm pull-up resistors (S1). The FDC chip used is the 1793 (IC 41) or equivalent which can handle 5.25-inch or 8-inch discs in single or double density, depending on the settings of two signals controlled from Port 1 (IC 34). The 74LS157 multiplexer (IC 31) is used to select the different signals for use with 5.25-inch or 8-inch drives. The links are pre-wired for a YE-Data separator but, to enable use with the SMC 9216B separator and BASF 610X drives, a set of links is provided to change the functions of some pins:

YE-data separator	link LK3 2-3, LK3 5-6, LK4 1-2
SMC 9216B	link LK3 1-2, LK3 4-5, disconnect LK4
For 5.25-inch drives:	
BASF 6106/6108	link LK3 8-9
YE Data YD 274	link LK3 7-8
For 8-inch drives:	link LK3 8-9

2. There are two types of data separator catered for in the design:

   - The YE-Data 3-chip set
   - The SMC 9216B single 8-pin device.

   The links required to operate with the two types are described above, but it is also necessary to remove the data separator chips that are not required. Therefore, for use with the YE-Data separator, remove the 9216 (IC 32); for use with the SMC 9216B, remove the MB4393 (IC 17), MB14323 (IC 26) and MB14324 (IC 33).

   The YE-Data separator also requires several other components, some of which should be of fairly close tolerance. The two monostable chains terminated by MONO8 (IC 24) and MONO5 (IC 25) require the first element to be within 5% of 2.5us and 5.0us respectively (i.e. 0.125us and 0.25us). The FDC chip requesting data is used to trigger the monostable, IC 21 (non-critical), which decreases the gain on the phase-locked loop (MB4393). The 100pF capacitor (C28) on pins 6 and 7 of the MB4393 sets the free-run frequency which should be close to 2MHz.

SECTION 6

INTELLIGENT DISC CONTROLLER BOARD

DIAGNOSTIC NOTES

How to Use these Notes

These notes look at the various problems that can occur and follow through a logical sequence to trace the fault. This may involve visual inspection of a particular section of the board or changing certain components to find the cause of the fault. On later boards most ICs are soldered directly into the PCB, so swapping of ICs is not advisable until a fault is definitely traced. This minimizes damage to the PCB. A logic probe would be useful in many places to quickly check that signals are at particular points and that they are not shorted high or low.

Use these notes in conjunction with circuit diagrams DC1/4 - DC4/4 and the board schematic diagram to help understand the fault-finding process.

All symptoms are listed below, and each is detailed on the following sheets (1-6).

Symptom

1. No COS prompt on power-up.
2. LED not on.
3. LED flashing FAULT 2.

3.1 LED flashing FAULT 3.
3.2 LED flashing FAULT 4.
3.3 LED flashing FAULT 5.
3.4 LED flashing FAULT 6.

4. LED on - no boot.
5. No boot - instant error message.
6. Long time to boot or does not quite boot.

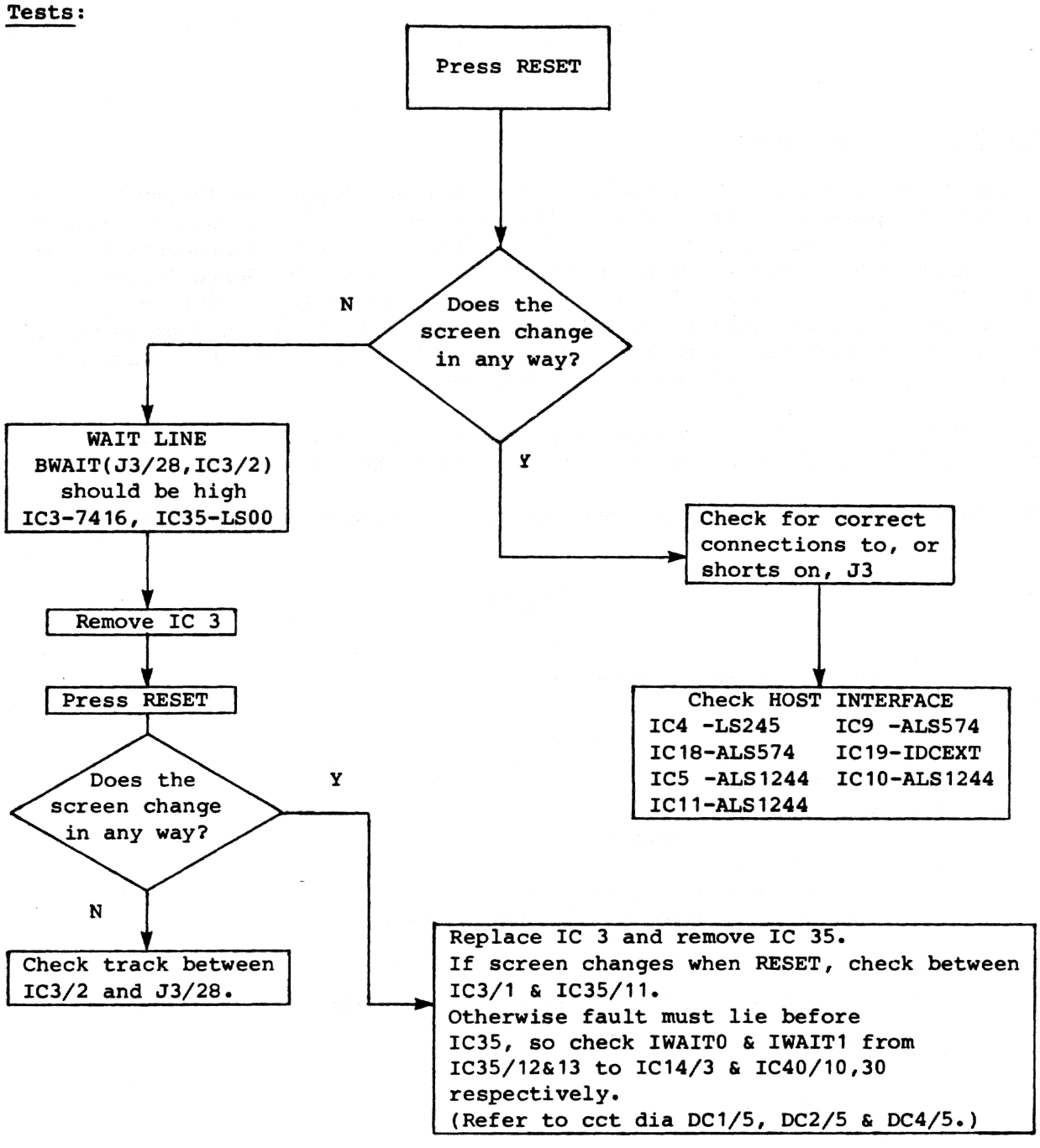
Additional notes are appended to this section covering the following:

- Use of IDCFLASH
- Use of ADDFLASH
- Further helpful hints
- Z80 signals
- Modifications.

IDC DIAGNOSTICS

Symptom 1: No COS prompt on power-up.

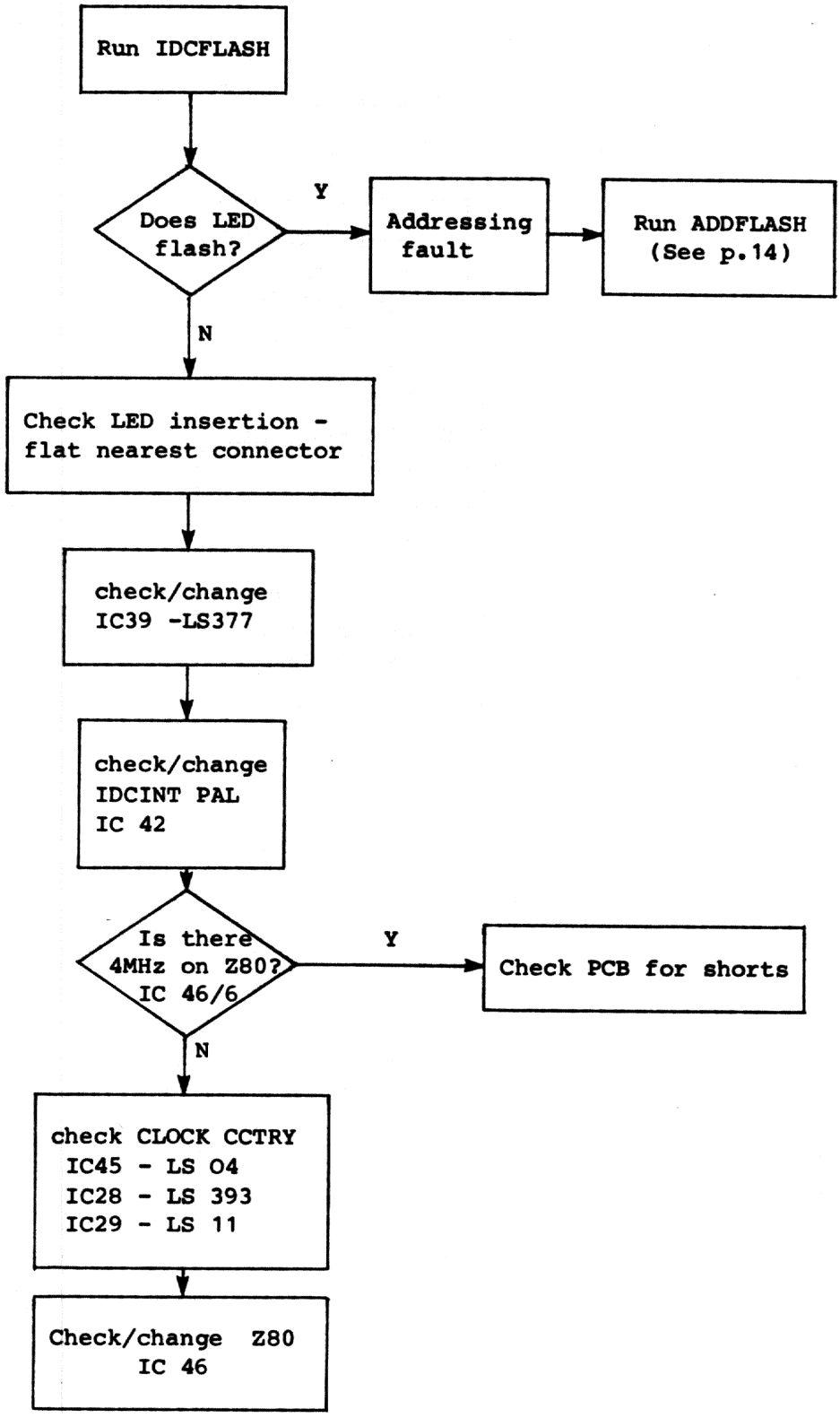
Tests:


Press RESET
Does the screen change in any way?
N
Y
WAIT LINE BWAIT(J3/28,IC3/2) should be high IC3-7416, IC35-LS00
Remove IC 3
Press RESET
Does the screen change in any way?
Y
N
Check track between IC3/2 and J3/28.
Check for correct connections to, or shorts on, J3
Check HOST INTERFACE
IC4 -LS245 IC9 -ALS574
IC18-ALS574 IC19-IDCEXT
IC5 -ALS1244 IC10-ALS1244
IC11-ALS1244
Replace IC 3 and remove IC 35.
If screen changes when RESET, check between IC3/1 & IC35/11.
Otherwise fault must lie before IC35, so check IWAIT0 & IWAIT1 from IC35/12&13 to IC14/3 & IC40/10,30 respectively.
(Refer to cct dia DC1/5, DC2/5 & DC4/5.)

IDC DIAGNOSTICS

Symptom 2 LED not on.

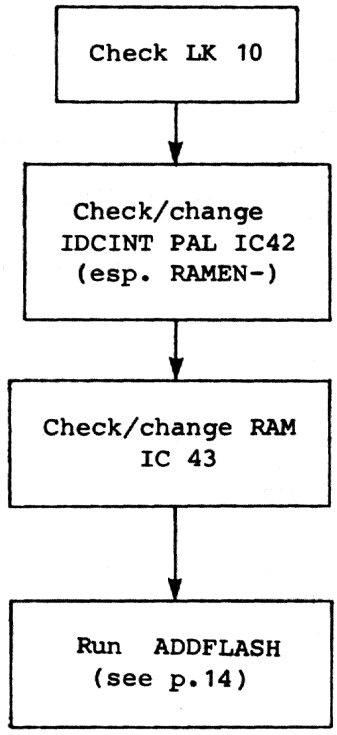
Tests :



IDC DIAGNOSTICS

Symptom 3 LED flashing, indicating 'FAULT 2' (RAM fault).

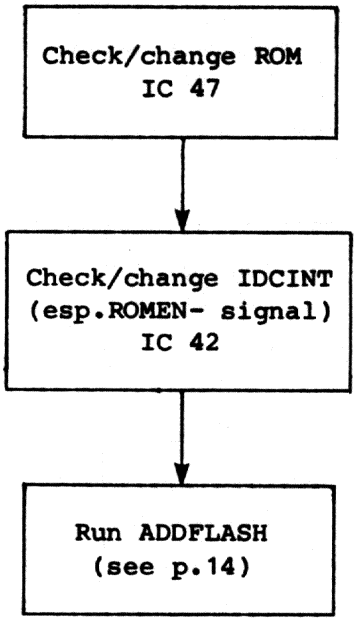
Tests :



IDC DIAGNOSTICS

Symptom 3.1 LED flashing, indicating 'FAULT 3' (ROM fault).

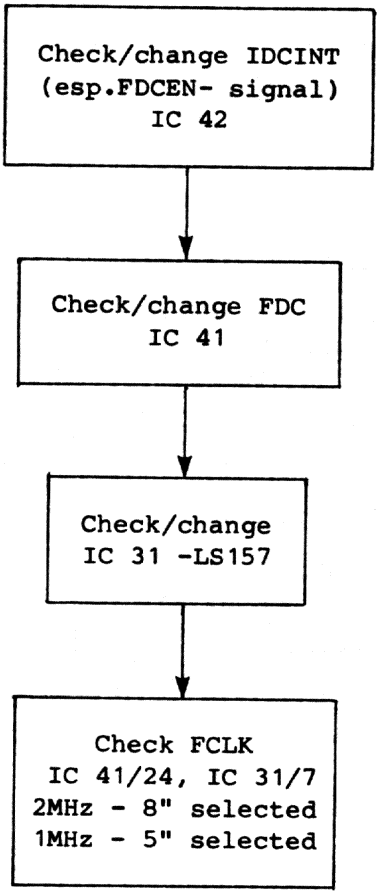
Tests :



IDC DIAGNOSTICS

Symptom 3.2 LED flashing, indicating 'FAULT 4' (FDC fault).

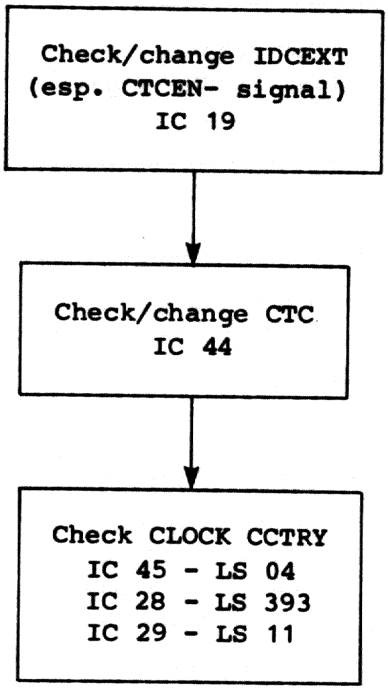
Tests :



IDC DIAGNOSTICS

Symptom 3.3 LED flashing, indicating 'FAULT 5' (CTC fault).

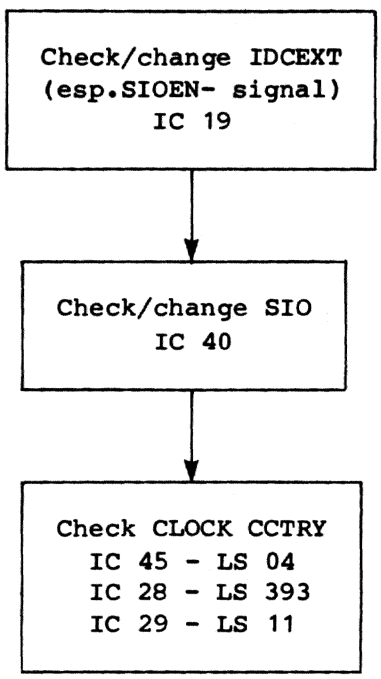
Tests :



IDC DIAGNOSTICS

Symptom 3.4 LED flashing, indicating 'FAULT 6' (SIO fault).

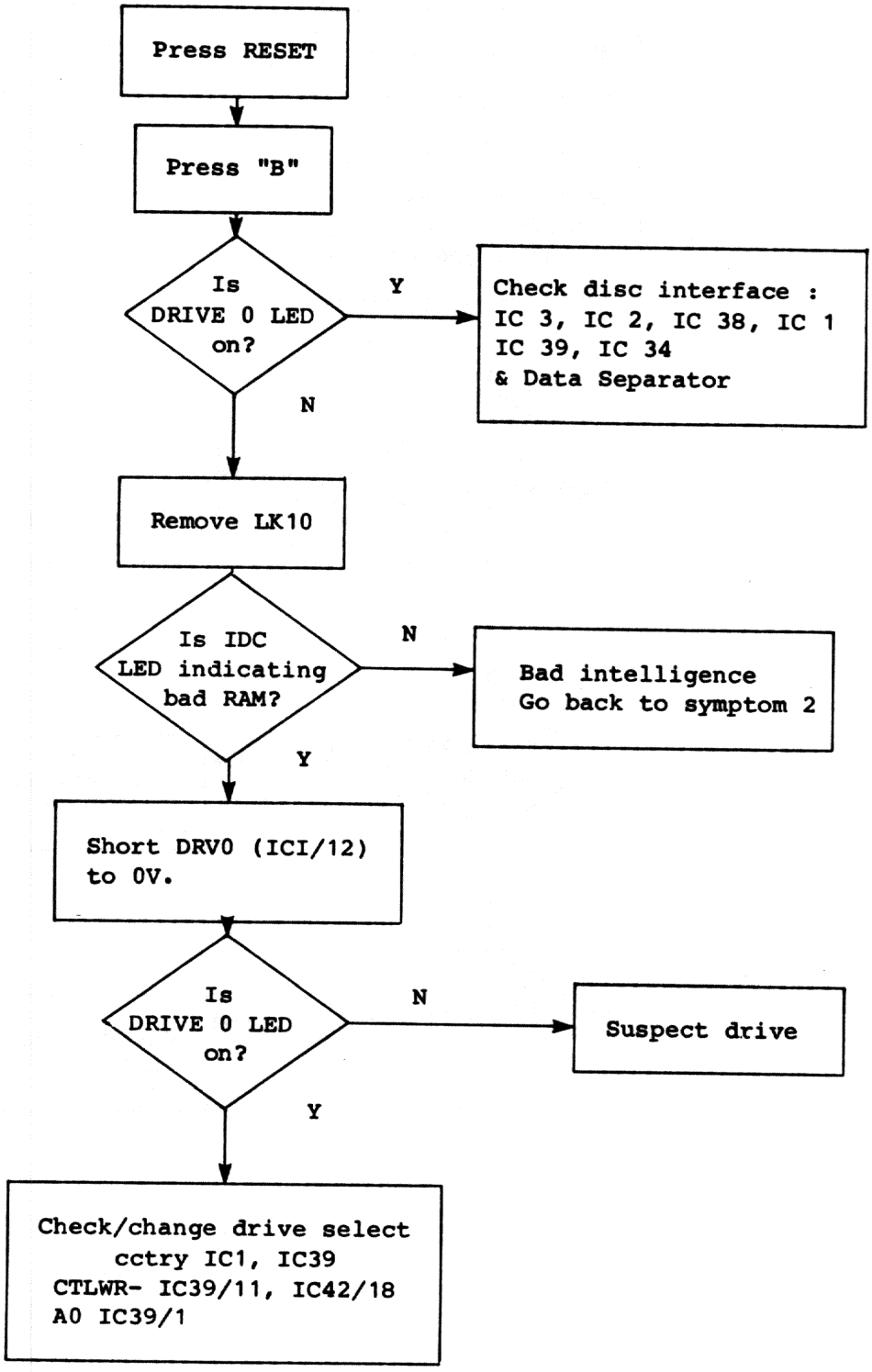
Tests :



IDC DIAGNOSTICS

Symptom 4 LED on, but system will not boot.

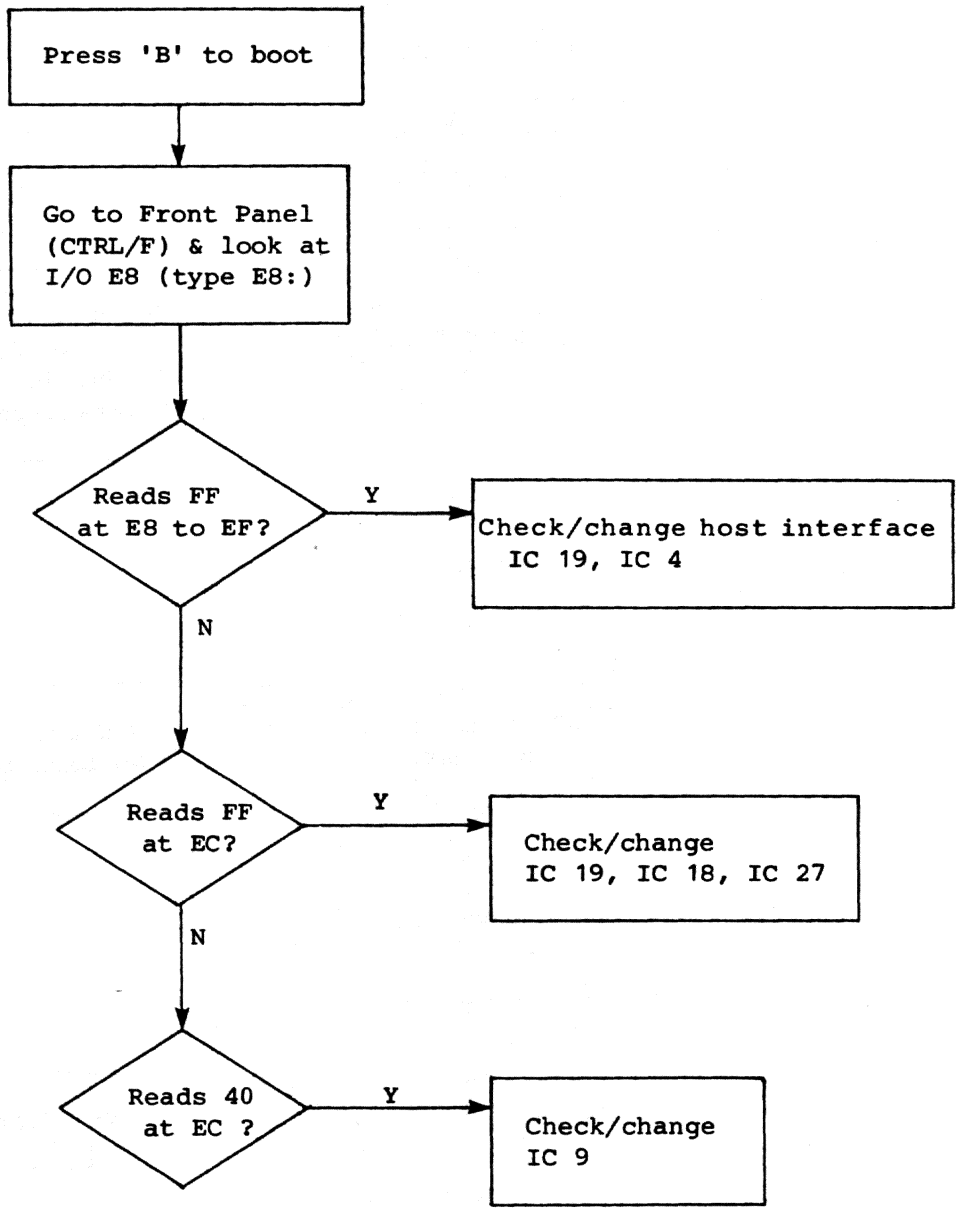
Tests :


Press RESET
Press "B"
Is DRIVE 0 LED on?
Y
Check disc interface : IC 3, IC 2, IC 38, IC 1 IC 39, IC 34 & Data Separator
N
Remove LK10
Is IDC LED indicating bad RAM?
N
Bad intelligence Go back to symptom 2
Y
Short DRV0 (ICI/12) to 0V.
Is DRIVE 0 LED on?
N
Suspect drive
Y
Check/change drive select cctry IC1, IC39 CTLWR- IC39/11, IC42/18 A0 IC39/1

IDC DIAGNOSTICS

Symptom 5 No boot - error message appears instantly (380Z only)

Tests :


Press 'B' to boot
Go to Front Panel (CTRL/F) & look at I/O E8 (type E8:)
Reads FF at E8 to EF?
Y
Check/change host interface IC 19, IC 4
N
Reads FF at EC?
Y
Check/change IC 19, IC 18, IC 27
N
Reads 40 at EC ?
Y
Check/change IC 9

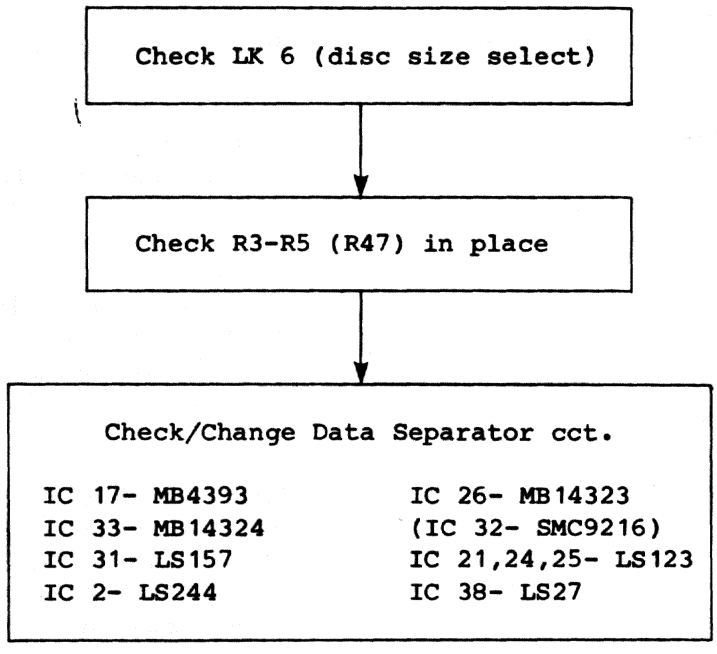
Other Symptoms:

SYMPTOM		CAUSE
Breaks to Front Panel on boot	-	Probably an unformatted disc.
380Z - <boot fault!> or <boot err!>	-	Wrong disc or no CP/M.
480Z - <drive not ready>	-	Could be faulty cable(s), faulty disc I/O buffers (IC 1, IC 2, IC 3, IC 8).
480Z - <boot error>	-	Could be faulty disc or bad data separator. (IC 17, IC 26, IC 33, IC 36, IC 31, IC 24, IC 25, IC 32)
480Z - <disc error>	-	Could be that the IDC is not communicating. Check SIO (IC 40, IC 6, IC 7, IC 15, IC 16) and intelligence. (Use tests in "Symptom 2".)
480Z - <?boot?>	-	Wrong or bad disc.

IDC DIAGNOSTICS

Symptom 6 System takes a long time to boot or does not quite boot.

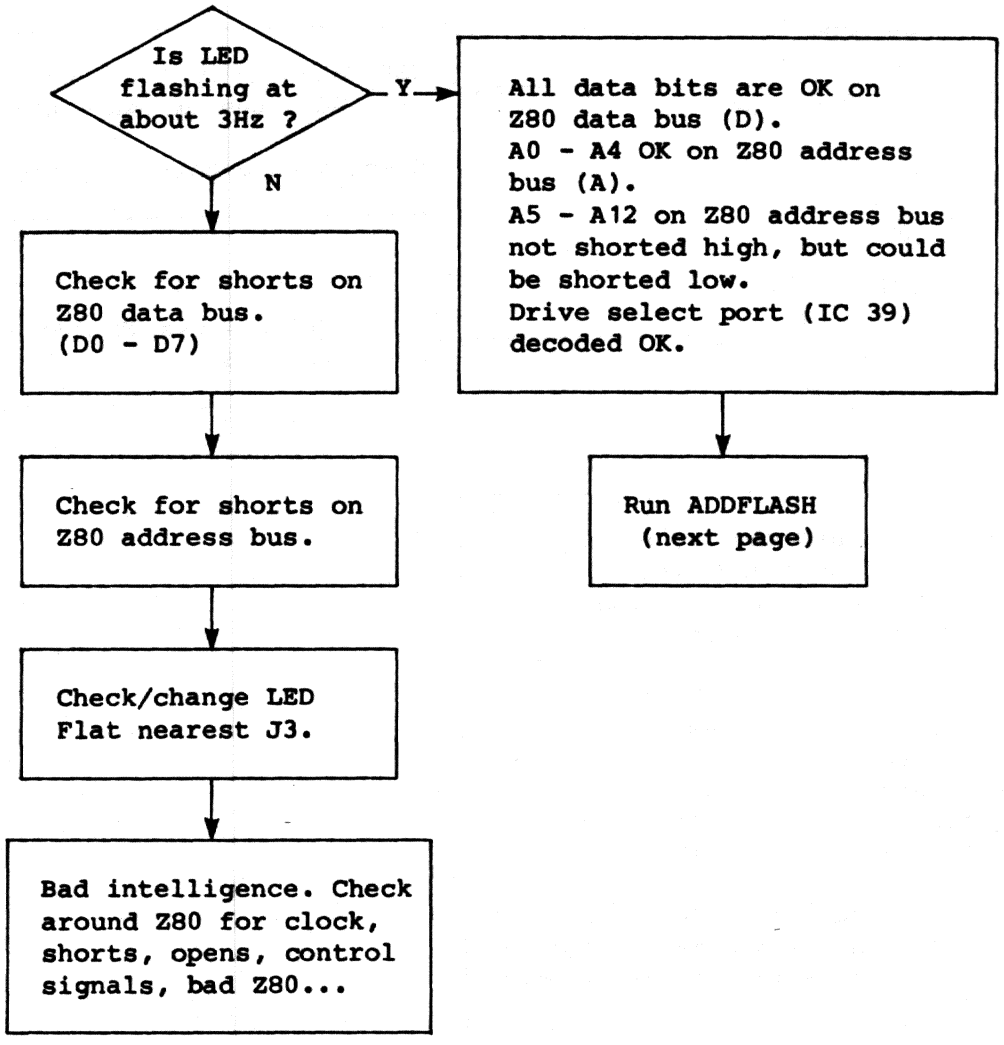
Tests :



IDC DIAGNOSTICS

Notes on the Use of IDCFLASH

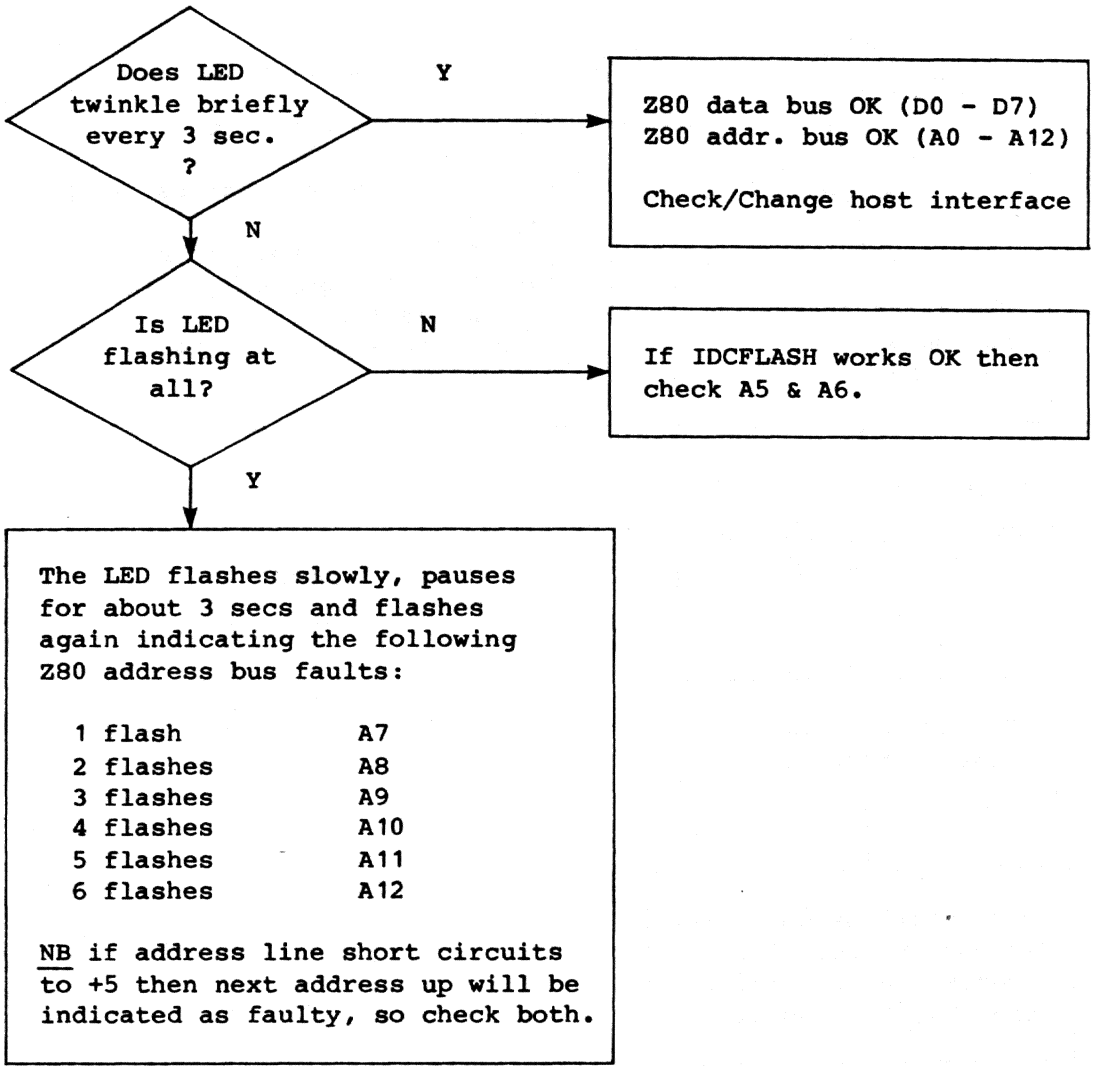
Insert IDCFLASH in ROM socket and switch on .....


Is LED flashing at about 3Hz ?
Y
N
All data bits are OK on Z80 data bus (D).
A0 - A4 OK on Z80 address bus (A).
A5 - A12 on Z80 address bus not shorted high, but could be shorted low.
Drive select port (IC 39) decoded OK.
Run ADDFLASH (next page)
Check for shorts on Z80 data bus. (D0 - D7)
Check for shorts on Z80 address bus.
Check/change LED Flat nearest J3.
Bad intelligence. Check around Z80 for clock, shorts, opens, control signals, bad Z80...

IDC DIAGNOSTICS

Notes on the Use of ADDFLASH

Insert ADDFLASH in ROM socket and switch on....


Does LED twinkle briefly every 3 sec. ?
Y
Z80 data bus OK (D0 - D7)
Z80 addr. bus OK (A0 - A12)
Check/Change host interface
N
Is LED flashing at all?
N
If IDCFLASH works OK then check A5 & A6.
Y
The LED flashes slowly, pauses for about 3 secs and flashes again indicating the following Z80 address bus faults:
1 flash A7
2 flashes A8
3 flashes A9
4 flashes A10
5 flashes A11
6 flashes A12
NB if address line short circuits to +5 then next address up will be indicated as faulty, so check both.

IDC DIAGNOSTICS

Further Helpful Hints

PALs: PALs control the selection of the various interface chips, so if a particular chip appears not to be working then the chip enable signal is a possible problem.

IDCEXT (white-purple-orange)
CTCEN-, SIOEN-, HWR-, HRD-, BDIR-

IDCINT (white-purple-yellow)
ROMEN-, RAMEN-, FDCEN0-, DWR-, DRD-, CTLWR-

Interrupts: A few devices on the IDC board generate interrupts which could interfere with the operation of the system. The SIO and the CTC put interrupts to the host, so if they start continually interrupting, the host gets tied up. This signal is IINT- and is found on IC 44/12, IC 40/5 and appears at J3/30 as BINT- after going via IC 1/3,4.

Links: Links are worth checking as these could prevent the system working:

- LK6 - select 5"/8" (link nearest edge of PCB for 8")
- LK9 - select ROM type (now pre-linked)
- LK10 - select RAM type (link nearest RAM for 2k RAM)

TTL: It is worth checking that there is no LS where ALS should be.

Clock: An LS04 is used rather than S04.
Check also that 1K2 resistors are used for R28,29.

Errors: Occasional errors in booting or read/write could be due to R3-R5 being missing or having the wrong value. They should be 47 Ohm.

Shorts: The most common places for shorts are where tracks go between IC pins, where there are through holes near IC pins, or where modifications have been done (especially decoupling capacitors on the back of the PCB lying across tracks).

IDC DIAGNOSTICS

Z80 Signals

The following signals are on the Z80 when IDCFLASH is used. A logic probe could be used to check these signals:

A7-13	1-3, 37-40	L
A0-6	30-36	I
A14,15	4,5	I
PHI	6	I
D0-7	7-10, 12-14	I
Vcc	11	H
INT	16	L
NMI	17	H
HALT	18	H
MREQ	19	I
IORQ	20	I
RD	21	I
WR	22	I
BUSAK	23	H
WAIT	24	I
BUSRQ	25	H
RESET	26	H
M1	27	I
RFSH	28	I
GND	29	L

H - high, L - low, I - changing

IDC DIAGNOSTIC

Modifications

The current modifications are:

FDS Join:

IC 39/12 to IC 21/3
IC 38/9 to IC 21/2
IC 41/20 to lower side C51
Upper side C51 TO IC 45/14

Cut:

IC 21/2 to IC 39/12
Under IC 21 to IC 21/3

Add 104 skycap:

IC 4/20 to IC 3/7
IC 28/14 to IC 28/2
IC 46/29 to IC 46/11

MDS Join:

As FDS + IC 12/11 to R26 (end near C48)

Cut:

As FDS + IC 12/11 to IC 28/13

Add:

As FDS.

SECTION 7

NETWORK TRANSCEIVER OPERATION

DESCRIPTION

A transceiver contains circuitry to encode and decode NRZI data, detect carrier and collisions, and to isolate the common bus from the station electronics and power supply. Data "modem handshake" lines, power, and an 8MHz clock are provided by the station. The station SIO transmits or receives a SDLC switched packet with a preamble and postamble of flags, as defined in the packet descriptions.

To transmit, the SIO asserts RTS and the transceiver asserts CTS, if there is no carrier detected. If there is a carrier detected, (i.e. a packet is being transmitted on the common bus) the CTS signal is delayed until the network is idle, provided RTS is not withdrawn. The transceiver provides an 800kHz clock to the SIO separate from the 8MHz clock. Data from the SIO to the transceiver is clocked on positive edges of the 800kHz clock and data from the transceiver to the SIO is clocked on negative edges. When CTS becomes true, the SIO will start transmitting the packet and, upon completion, will remove RTS. If a collision is detected, the transceiver must negate CTS and jam the network with a logic 1 to ensure that other transceivers detect the collision. RTS will be negated by the SIO in response to the collision detection.

The transceiver contains a 'watchdog' monostable which is re-triggered by RTS and which is used to limit the transmission time of the transceiver to the maximum packet length. The watchdog period has been set to 30us on Research Machines' transceivers to allow for future use of 2K packets. The transceiver may only transmit onto the common bus while RTS and the watchdog are asserted.

When not transmitting, the transceiver is in receive mode, constantly monitoring the common bus. When packets are detected, the transceiver synchronises the 800 kHz clock to the received clock and provides this and the received data to the SIO. When the common bus is idle, the transceiver must provide a logic 1 data level to the SIO.

DTR is used as a test mode signal. When asserted by the SIO, the transceiver should assert DCD to show its presence. When DTR is asserted and a collision is detected on the common bus between two other transceivers, DCD should be negated for the duration of the collision.

Collision signals should not be generated by a transceiver in receive mode disconnected from the common bus cable.

To disable an internal transceiver, Research Machines' external transceivers should ground the 'transceiver present' line on the network interface.

380Z NETWORK INTERFACE BOARD

This board is a multi-purpose board and may be configured either as a Network Interface Board (NIB) or as a Dual Serial Interface Board. The relevant circuit diagrams are :-

380Z-NET-1 Version I 30th March 1982
380Z-NET-2 Version F 30th March 1982
380Z-NET-3 Version H 30th March 1982
380Z-NET-4 Version B 30th March 1982

In this configuration, as a Network Interface Board, it will upgrade a standard 380Z into a network server when used in conjunction with a 380Z Internal Transceiver Board or an external transceiver.

The serial interfaces are based around the dual-channel Z80-SIO which is capable of operating under various asynchronous and synchronous protocols at baud rates not exceeding 800kHz. Both channels are capable of polled or interrupt-driven operation, or operating under DMA or wait-state control. Channel A is hard-configured to be a network interface port and Channel B as an RS232 serial port.

The SIO may be supported by a Z80-DMA which can be triggered by either of the SIO channels under programmable, or soldered DIL, header selection. The DMA is fully buffered to the Z50 bus and is expandable to allow multiple DMAs in the 380Z. The DMA may be programmed to support transfers between the SIO and memory, or memory and memory, within the 380Z. DMA support is an option not normally required, the Z80-DMA IC is omitted and the link "DMAL" connected.

Baud rate generation is supported by a Z80-CTC and standard rates of up to 38k4 baud may be used. Channel A of the SIO has links to select the send and receive baud rates. Link A selects the receive rate between CTC2 channel 0 or the transmit rate; link B selects the transmit rate between CTC2 channel 1 or the externally provided network clock rate. Channel B baud rate is controlled by CTC2 channel 2.

CTC1 is available for general system timing. An 8-bit switch register, as a read-only I/O port, is provided for power-up option use.

The Network Interface (J3)

(Circuit : NET-2)

This is based on an SIO channel operating in SDLC mode at the maximum clock rate (800kHz). Data In and Out, Clock In and Out, RTS, CTS, DTR and DCD are buffered and taken (via a ribbon cable) to either:

- a 15-way Cannon D-type connector mounted on the rear panel

or

- an Internal Transceiver Board.

+12V DC is also provided to the interface to power the transceiver. A

multi-way cable, up to 30 feet long, connects the computer to the external transceiver. Collision status is monitored by the CTS modem input. Tx Enable is controlled by the DTR modem output.

RS232 Interface (J2)

(Circuit : NET-2)

This is similar to the current SIO-4 but with improvements. Standard data rates of 38k4 and 19k2 baud can be accommodated. The interface may be driven by polled, interrupt, or DMA operation. All the signals go via a DIL header position (Header C) to a 20-way header, and to the rear panel via a "User I/O Cable". This is a cheaper and more robust alternative to the current "SIO-4" cable. All signal and modem handshake reallocations are dealt with at the DIL header position, thus avoiding the normal confusion regarding soldering cables. The header position is prewired for normal DTE operation. To convert to DCE operation, the PCB links should be cut and pin pairs: 1-14, 2-13, 3-12, 4-11, 6-9 and 7-8 should be wired together.

Header C:

SIO Channel B					RS232 signals
	TxD	1	14	BA	
	RxD	2	13	BB	
	RTS	3	12	CA	
	CTS	4	11	CB	
		5	10	CC	
	DTR	6	9	CD	
	DCD	7	8	DF	

Timing

There is an on-board 16MHz crystal oscillator for all timing. This is divided by 26 in hardware to produce a master "times sixteen" baud clock (615kHz) from which all baud clock rates are derived by CTC channels. All CTC triggers and zero counts are taken to a DIL header position together with the master baud clock and another divided-down signal (600Hz).

CTC1 is intended for system timing interrupts (1ms, 2ms and 20ms). The most usual configuration will be prewired, but is easily changed by cutting PCB links and soldering a DIL header in Header B position.

Header B:

	CTC1				CTC2
	Tr0 *	1	16	Tr0 **	
	ZC0	2	15	ZC0	
	Tr1 *	3	14	Tr1 **	
(	ZC1	4	13	ZC1	
cascaded (	Tr2	5	12	Tr2 **	
(	ZC2	6	11	ZC2	
(	Tr3	7	10	Tr3	
	600Hz	8	9	Baud Clock (615kHz)	

* prewired to 600Hz

** prewired to baud clock

Interrupts

Full-standard, priority daisy chain patching has been implemented which is compatible with all recent 380Z boards (Red = BIEI, Black = BIEO). If other boards operating with interrupts are used, the daisy chain must be connected using the interrupt patch cable provided with the board. The on-board priority is prewired at a DIL position, but may be changed by cutting the PCB links and using a DIL header. The default priority order (highest first) will be:

SIO, DMA, CTC1, CTC2

Header A:

CTC2EO	1	14	
CTC1EO	2	13	CTC2EI
DMAEO	3	12	CTC1EI
SIOEO	4	11	DMAEI
BIEI	5	10	SEOEI
	6	9	
DMAEO	7	8	DMAEI

DMAEO and DMAEI are shorted with a prewired link between pins 7 and 8 of Header A. If the DMA is installed this link must be cut.

Mapping

All ports are I/O mapped and controlled by a PAL. The CTCs (8 ports), the SIO (4), the DMA (1 port), switch register (1) and control port (1) are all mapped from D0H to DFH - in between the two standard FDC blocks. The PAL is designated a number, PDn, where n shows the mapping configuration. The current correct version is PD7, revision C (Red/Violet/Yellow).

DF	Switch Register (Read Only)
DE	Control Port (Write Only)
DD	Switch/Control (R/W)
DC	DMA
DB	SIO-B Control
DA	SIO-B Data
D9	SIO-A Control
D8	SIO-A Data
D7	CTC2 Channel 3
D6	CTC2 Channel 2 (SIO-B baud rate)
D5	CTC2 Channel 1
D4	CTC2 Channel 0
D3	CTC1 Channel 3
D2	CTC1 Channel 2
D1	CTC1 Channel 1
D0	CTC1 Channel 0

DMA Controller (omitted on standard board)

(Circuit : NET-1)

When the DMA controller is installed, two preset links must be cut: one in the interrupt daisy chain and the other in the bus-acknowledge daisy chain.

A bus acknowledgement priority daisy chain has been introduced, to enable multiple DMA controllers in one 380Z (or server). BBAI (Yellow) and BBAO (Blue) 2mm patch sockets are provided for cascading, and are similar to the Red and Black ones already in use for interrupt priority patching. A link is provided to connect BUSAK from the Z50 bus to the top of the daisy chain, and this must be connected on the first (or only) board in a DMA system.

Wait states are introduced on MREQ cycles when the DMA has control of the bus to make memory timing the same as the CPU. The Wait/Ready signals from each SIO channel are routed to either the Wait line or the DMA ready input under the control of seven bits in the control port register.

Programming the Control Port (omitted on standard board)

The WRSx signals control the Wait/Ready selection: Bit 6 is an enable and bits 5 to 0 select any of the 32 possible combinations of SIO channels A and/or B operating under Wait-state or Ready-triggered modes. The selections are in a PROM, but for fixed non-programmable operation a DIL header may be substituted for the PROM. Wait/Ready A and Wait are connected by a preset cutable link on the standard board.

Wait/Ready Header:

	1	16	
	2	15	
	3	14	
	4	13	
W/R A	5	12	Ready
W/R B	6	11	Wait
	7	10	
	8	9	

Programming the SIO and DMA

The SIO and DMA devices are treated as a series of internal registers accessible through one I/O port address. Each SIO channel occupies two ports: data (read/write) and control (seven write registers and three read registers). However, these are non-symmetrical with certain parts being common to both channels. The DMA occupies one port through which all 21 internal registers are accessed by sequences; the maximum length is five operations. Care should be taken in the initialization and programming of these devices, and the use of tables is preferred in all but the most time-critical applications.

The SIO can produce up to eight vectored interrupts (four per channel). In order of priority these are:

- Special Conditions (Receive overrun, End of frame, CRC error)
- Receive Character Available
- Transmit Buffer Empty
- External Status Change (CTC, DCD or Synch status change, Break/Abort detection, or CRC detection)

Channel A has priority over Channel B.

The DMA can produce four vectored interrupts:

- On Ready (before Bus Request)
- On Match (with a data byte)
- On End of Block
- On Match and End of Block.

Programming the CTC Baud Rate

When the CTC triggers are connected to the baud clock, standard baud rates may be generated by simple division ratios. The control bytes and time constants to provide standard rates are as follows:

```
07H     142     ; 110 Baud
47H     0       ; 150 Baud
47H     128     ; 300 Baud
47H     64      ; 600 Baud
47H     32      ;1200 Baud
47H     16      ;2400 Baud
47H     8       ;4800 Baud
47H     4       ;9600 Baud
47H     2       ;19k2 Baud
47H     1       ;38k4 Baud
```

The relevant byte pair should be loaded to CTC2 channel 2.

CONNECTORS

J1: RS232C Interface — 3M Header

AA	1	2	
BA	3	4	
BB	5	6	
CA	7	8	
CB	9	10	
CC	11	12	
AB	13	14	CD
CF	15	16	
	17	18	
	19	20	

J3: Network Interface — 3M Header

Clock Out (8MHz)	1	2	0V
Clock In (800MHz)	3	4	0V
TxD	5	6	0V
RxD	7	8	0V
RTS	9	10	CTS
DTR	11	12	DCD
+12V	13	14	Transceiver Present
+12V	15	16	Chassis

J4: Z50 BUS — 3M Header

BRESET-	1	2	BPAGE
BD0	3	4	BD1
BD2	5	6	BD3
BD4	7	8	BD5
BD6	9	10	BD7
BA0	11	12	BA1
BA2	13	14	BA3
BA4	15	16	BA5
BA6	17	18	BA7
BA8	19	20	BA9
BA10	21	22	BA11
BA12	23	24	BA13
BA14	25	26	BA15
BUSRQ-	27	28	BWAIT-
BUSAK-	29	30	BINT-
BNMI-	31	32	BHALT-
BIORQ-	33	34	BWR-
BRD-	35	36	BMREQ-
BRFSH-	37	38	BM1-
0V	39	40	BCLK (4MHz)
+5V	41	42	+5V
+5V	43	44	+12V
+5V	45	46	-12V
0V	47	48	0V
0V	49	50	0V

J5: BBAI 2mm Yellow (omitted on standard board)

J6: BBAO 2mm Blue (omitted on standard board)

J7: BIEI 2mm Red

J8: BIEO 2mm Black

The standard configuration Network Interface Board is populated with the following ICs only:

AP	74LS244
AQ	omit
AR	898-3-R330
AS	74LS244
AT	omit
AU	omit
BP	74LS244
BQ	omit
BR	74LS245
BS	omit
BT	omit
BU	75188
BV	75189
CP	PAL14L4 DMALOGc (Red/Violet/Green)
CQ	PAL10L8 PD7c (Red/Violet/Yellow)
CR	omit
CS	Z80A-SIO/0
DP	74LS32
DQ	74S04
DR	74LS244
EP	74LS74
EQ	74LS244
FP	74LS123
FQ	74L07
FR	Z80A-CTC
FS	Z80A-CTC
FT	omit
FU	DIL switch
GQ	74LS161
GR	CD4040
GS	74LS30
GT	omit
GU	omit
GV	omit
GW	omit
GX	74LS04

Power Supply Consumption (typical)

+5V	500mA
+12V	10mA
-12V	15mA

480Z HARDWARE

Mapping

All ports are I/O mapped and controlled by a PROM (JS):

18	Switch Register
24	SIO-A Data
25	SIO-B Data
26	SIO-A Control
27	SIO-B Control

Transceiver Connection

Early 480Zs have a pair of DIL sockets for connecting a 'piggy back' transceiver board.

NET2:	+12V (isolated)	1	14	0V (isolated)
		2	13	
	-12V	3	12	+5V
	0V	4	11	8MHz
	800kHz	5	10	IN2
	IN1	6	9	Wait-
	OUT0	7	8	SWait-
NET1:	RxD	1	14	RxC
	TxC	2	13	TxD
	DTR	3	12	RTS
	CTS	4	11	DCD
		5	10	
		6	9	
		7	8	8MHz

380Z Transceiver/NIB Connecting Cable

For using a 480Z Transceiver with a 380Z Network Interface board:

8MHz	1	---	J2-8
0V	2		
800kHz	3	---	J2-14
0V	4		
TxD	5	---	J2-13
0V	6		
RxD	7	---	J2-1
0V	8		
RTS	9	---	J2-12
CTS	10	---	J2-4
DTR	11	---	J2-3
DCD	12	---	J2-11
+12V	13		
+12V	14		
Trcv Present	15		
Chassis	16		

SECTION 8

HOST INTERFACE BOARD

INTRODUCTION

This section describes the low-level hardware operation of the Host Interface board (HIB). The design objectives are considered first, followed by the general description and use of the different on-board modules.

DESIGN OBJECTIVES

When Research Machines decided to look into winchester systems, the most convenient method of interfacing to the 380Z was via the IEEE interface. This was mainly due to availability and cost of winchester drives. The first non-released systems were using 8-inch IMI winchesters with an IEEE interface. The introduction of the network system showed the full potential of the winchester, and cost and speed of access led to deeper research of the winchester market. The introduction of the 5.25 inch high-capacity winchester brought a reduction in cost. A more convenient standard interface, the SASI (Shugart Associates System Interface) was introduced to interface to the new generation of winchesters. This meant that a new board would have to be designed in order to interface the 380Z to SASI. This new board would also have to work in a heavily interrupted environment and at high data transfer speed. The hardware had to be readily available and also of relatively low cost.

The MK1 HIB was therefore introduced with extra options, namely an Option Boot ROM, 16K by 8 Static RAM, and DMA. It was soon realised that the options were adding to the cost and no real use could be found to justify the extra cost on a server. Although MK1 HIB boards went into production, no options were fitted and the basic board design was not changed. The MKII HIB has minor differences to MKI and IC positions are indicated by numbers instead of letters. (Both sets of circuit diagrams, for MkI and MkII, are included with this section).

THE HARDWARE MODULES

The HIB circuit consists of a few hardware modules together with some logic to interface the various modules. Particular attention is paid on grounding the HIB to SASI. The modules are as follows:

- Bus Interface : To connect the HIB to the 380Z bus.
- Bus Decoding : To decode I/O and memory-mapped ports.
- Memory : The on-board RAM.

PIO chip
SASI data
SASI control
SASI termination

A full description of these modules is given below.

Bus Buffering

The address bus is buffered by three SN74LS1244N ICs (AA, AB, and AC) and the data bus by IC AF (SN74LS1245N). The BRFSH- signal is buffered by one segment of an inverter, IC AK (SN74LS14N) and outgoing signals BWAIT- and BINT- are buffered by an open collector, IC AL (SN7407N). Priority daisy chain interrupt is serviced by two segments of IC AI (SN74LS10N).

Bus Decoding

The decoding is done by two 12-input 6-output PAL 12L6 ICs (AD and AE). Addresses A0 to A7, together with control signals IORQ-, WR-, RESET- and M1- are used to produce decoded signals (through PAL IC AD) PIOM1-, PIOEN-, MCONTROL- and IORD-. For IC AE, addresses A9 to A15 are used together with control signals M1-, MREQ- and RFSH to produce decoded signals MEMRD- and DBMEMEN- (DBEN-). Not all decoded signals are mentioned because they are concerned with the original design options. Functions of decoded signals are as follows:

PIOM1- : This signal (apart from the M1 cycles to the PIO) acts as a PIO reset, when RESET- is present.

PIOEN- : Enables PIO for reading or writing.

MCONTROL- : Enables the four most-significant bit (MSB) addresses for the on-board memory. The four MSB addresses are under software control and the processor will set data bits D2 to D5 accordingly. IC BD (SN74LS273N) latches signals BANK2 to BANK5 at the end of the MCONTROL- cycle (low to high transition).

IORD- : When this signal is active, PIO is read and signal BUFDIR- is active thus pointing data bus direction to the 380Z bus.

MEMRD- : Indicates that on-board RAM is read by the 380Z and that BUFDIR- is active.

DBMEMEN- : Enables on-board RAM for read/write operations. This signal is fed through an OR gate and becomes DBEN-.

'Interrupt acknowledge' is taken care of by ICs AJ (SN74LS02N) and AH (SN74LS10N). BUFDIR- will be active when the HIB is in the process of an interrupt acknowledge or when the 380Z is reading either the on-board RAM or the PIO. The following table shows the mapping of the different ports on the HIB:

40H: PIO channel 'A' data	read/write
41H: PIO channel 'B' data	read/write
42H: PIO channel 'A' control	read/write
43H: PIO channel 'B' control	read/write
45H: PIO Deblocking RAM control	write only

F800 to F9FF Deblocking RAM memory space.

Memory

The on-board RAM, otherwise known as the deblocking RAM, is an 8K by 8 pseudostatic RAM D2186 (IC BG). Deblocking RAM occupies 512 bytes of memory space so it cannot all be read at once; the 380Z supplies the four MSB addresses BANK2 to BANK5 thus allowing RAM to be read or written in 1/2K chunks. This type of RAM is like the dynamic RAM but produces its own internal refresh cycles. If RAM is selected (by DBEN- going 'low' during an internal refresh cycle) pin 1 will go 'low' and a WAIT will be put onto the bus. Some types of 8K static RAM may also be used, such as the Toshiba type as used on the IDC.

Interface to SASI

The PIO IC, CA, is the primary unit for interfacing to SASI. It handles data and commands through channel 'A' and control signals from and to SASI through channel 'B'. Address line A0 is used to select the appropriate channel for data transfer between Z80A-CPU and Z80A-PIO, whilst address A1 defines the type of data transfer to be performed, i.e. data or command.

Although channel 'A' uses all 8 bits in bi-directional mode, channel 'B' bits BD0, BD1, BD2, BD3, BD6 and BD7 are used as inputs whilst BD4, and BD5 bits are used as outputs. The bus clock is fed through one segment of IC AL, an open collector buffer, with the output pulled up by a 330 Ohm resistor, to produce ZCLOCK for the PIO.

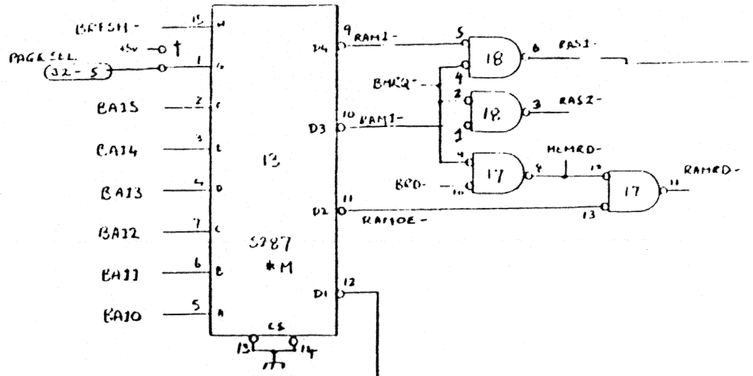
Data transfer between PIO and SASI is done via IC CB, an open collector bus transceiver (SN74LS642-1N).

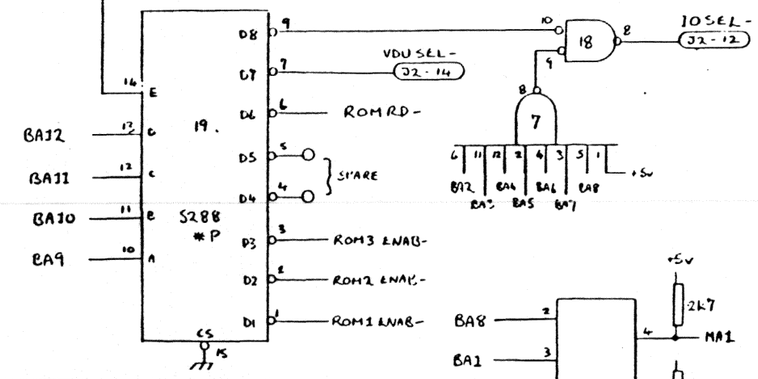
Control to and from SASI is more complicated due to the handshaking procedure. Direction of the bus transceiver is under SASI control by signal IN, but enabling will not take place at the correct time unless control signals are allowed to settle down. This is achieved by taking the acknowledge signals, i.e. select, read, and write, and delaying them by a predetermined factor, thus allowing good set-up times. The delaying takes place at IC CC (SN74LS273N) by connecting one output to the next input and clocking them through using the 4MHz clock. WRACK is delayed by a factor of two, thus becoming WRACKDEL, whilst RDACK and SELACK are delayed by a factor of three and so becoming RDACKDEL and SELDEL. IC CC is continuously reset through IC CF (SN74LS02N) by signal REQ or WRACKDEL or RDACKDEL but also allowing for a reset from the Z50 bus.

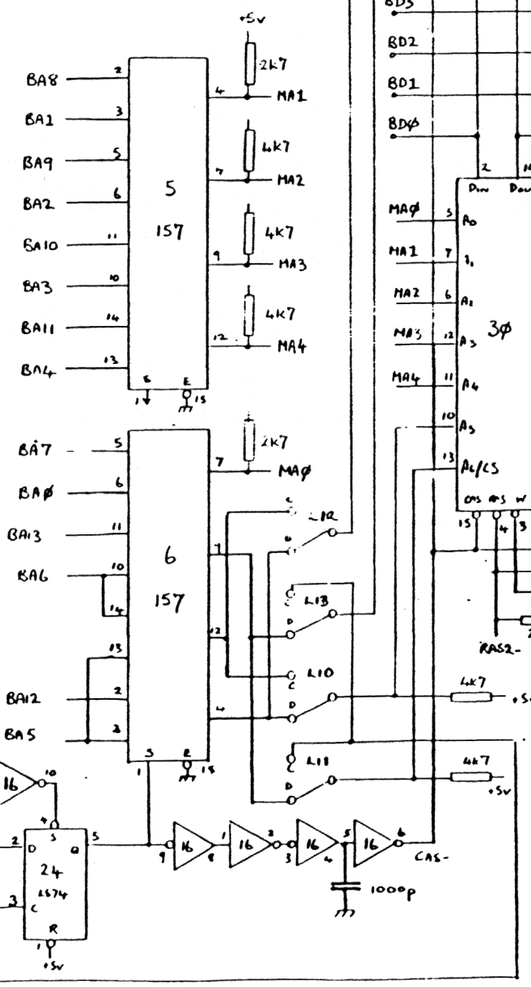
The SASI bus transceiver is enabled by signal SDBUFEN- in both directions. SELACK or WRACK enable IC CB when IN signal is 'low' (pointing to SASI) and

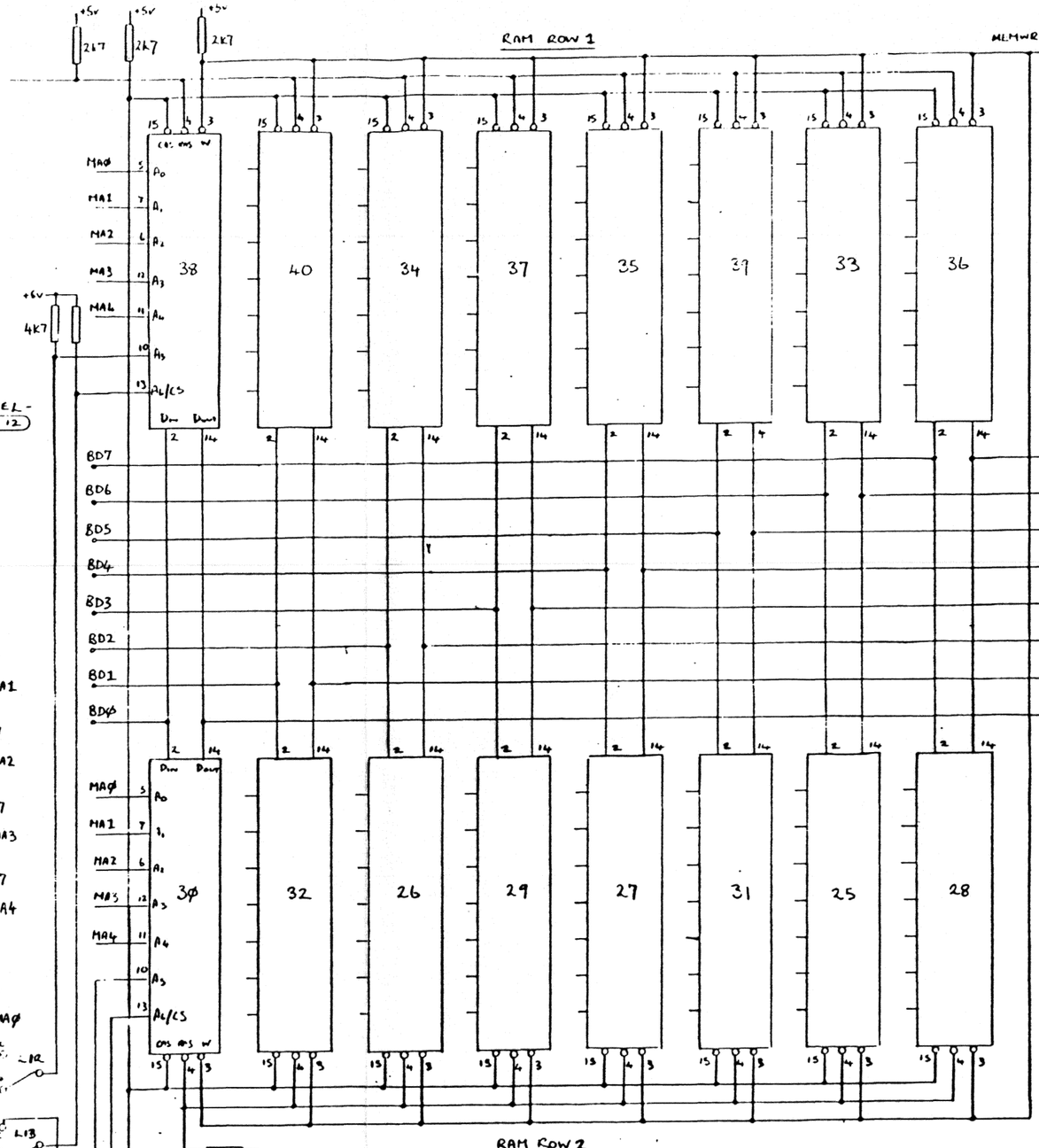
RDACK or RDACKDEL enable IC CB when IN is 'high' (PIO reading from SASI). WRACKDEK and RDACKDEL are supplying the acknowledge signal to SASI.

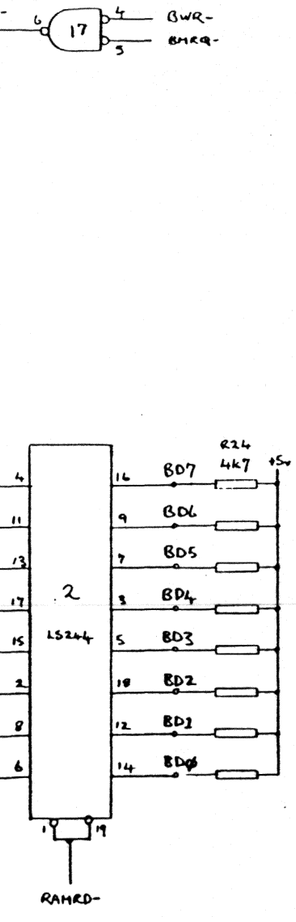
Termination is done at both sides of the transceiver (open collector outputs) by using a 4K7 resistor network, RB, at the PIO side, pulling the bus to +5V, and by a pull-up resistor network, RC (150 Ohm resistors) at SASI side and connecting to a 2.9V terminating voltage. Terminating voltage is derived using a three diode chain connected to ground by R2 (0.7V drop across each diode). Particular attention is taken for grounding SASI control signals: a 0.56 Ohm resistor is connected between SASI ground and HIB ground for ground noise elimination.

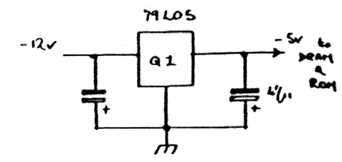












*M MEMORY MAP PROM		
BOARD	IC 33	COLOUR CODE
C4100 4K/8K	A	—
C4100 20K	M3	—
C4100 16K/32K	M4	—
C4100 ADDON RAM	M5	—
C100 32K only C100 32K ADD ON RAM	M7	BLUE
	M8	RED
C100 16K/32K	M9	VIOLET
C100 20K	M10	RED/YELLOW
P.O SPECIAL 62K	M11A	—

† WIRE LINK TO +5V ON ADD ON RAM

L10 & L11 , L12 & L13
C - 4K DRAM 4027
D - 16K DRAM 4116
EACH ROW MAY BE 4K or 16K
FOR 20K BOARDS ROW2
MUST BE 16K

*P PORT MAP PROM
ADD ON RAM — NOT USED
MONITOR C100
2 × 2716 P5 WHITE
2716 + 2×2708 P6 ORANGE
MONITOR C4100
2 × 2716 P3
2716 + 2×2708 3

17-12-79	380Z: CPU/RAM (ALSO ADD ON RAM)
2 8-2-80	
3 13-6-80	
	© 1977, 1979 DRAWING 1
	RESEARCH MACHINES LTD

PORT3 RD-

LS244

LS374

PORT3 WR-

BD7 BD6 BD5 BD4 BD3 BD2 BD1 BDØ

USER I/O

ROM3 2708 or TMS2716 41

ROM2 2708 or TMS2716 42

ROM1 2708 or TMS2716 43

ROM3 ENAB-

ROM2 ENAB-

ROM1 ENAB-

ROM LINKS
2708 —o
2716 —o

ROMRD-
MEMRD-

LS 244

DATA BUFFER OUT -

LS241

BD7 BD6 BD5 BD4 BD3 BD2 BD1 BDØ

R1 4K7

R4 4K7

R5 4K7

Z80A-CPU

BHLT- J3-32
BINT- J3-30
BREQ- J3-27
BNMI- J3-31
BWAIT- J3-28
BUSAK- J3-29
BRESET- J3-1
RESET+ J2-9

M1- NMI ENABLE J2-6

BA15 J3-26
BA14 J3-25
BA13 J3-24
BA12 J3-23
BA11 J3-22
BA10 J3-21 J2-34
BA9 J3-20 J2-33
BA8 J3-19 J2-32
BA7 J3-18 J2-31
BA6 J3-17 J2-30
BA5 J3-16 J2-29
BA4 J3-15 J2-28
BA3 J3-14 J2-27
BA2 J3-13 J2-26
BA1 J3-12 J2-25
BAØ J3-11 J2-24

BRFSH- J3-37
BIORQ- J3-33
BWR- J3-34
BRD- J3-35
BM1- J3-32 J2-3
BMRQ- J3-36
BCLK J3-40

M1.RD+

4MHz

A - WAIT STATE EVERY MEMORY CYCLE
B - " " " M1 CYCLE

1	11-12-79 GShutt
2	14-1-80
3	8-2-80
4	25-2-80
5	25-4-80

380Z: CPU-2

CPU, ROM, USER I/O, TIMING AND BUS BUFFERING

DRAWING 2

RESEARCH MACHINES LTD

VIDEO MEMORY

ROW-COLUMN ADDRESS REMAPPING

= 26 WAY TRANSITION TO CPU BOARD

1	9-12-79	D12690 Sht 1 of 2
2	13-2-80	380Z : VDU-1
3	29-2-80	KEYBOARD & CASSETTE INTERFACES
4	5-6-80	PORTS & VIDEO MEMORY
5	10-08-84	DRAWING 1

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RESEARCH MACHINES LTD

38	LS32
39	LS02
40	LS11
41	LS04
43	LS12

RC0 RC1 RC2 RC3 — 40, 38, 39, 38, 38

MD1 MD5 MD3 MD0 MD6 MD7 MD4 — 35 LS153

42 LS174 — +5V CLR, CLK; MD6, MD7; GREY-; GRAPHICS+

41, 43, 39, 25 — VIDEO MIX; WHITE INHIBIT; VDU ON+; VDU ON-

R24 2K7; R27 3K3; R30 3K3; R31 1K8; R32 1K8; C15 82P; VIDG; VIDW

25 — LINE BLANKING

MD0 MD1 MD2 MD3 MD4 MD5 MD6 — 27 S262 — RA RB RC RD; RC2 RC3

28 LS174 — FRAME RESET

29 LS151 — CC0 CC1 CC2

R26 560R; IN6148 D1 D2; R25 2K7; -6V

R36 8K9; R28 180R; D3 9V1; Q2 2N3704; R29 180R; VIDEO OUTPUT; R34 470R; R33 180R; +9V; R35 180R; +RV

"2" - GREEN LINE WAVEFORMS 31 6287 — D4 D3 D2 D1; CS; FRAME SWITCH

34 LS75 — LINE SYNC; LINE BLANKING; LINE COUNT

"D" - YELLOW FRAME WAVEFORMS 36 5287 — D1 D2 D3 D4; FRAME BLANKING; FRAME SWITCH; FRAME ACCESS

LINE ACCESS

CC0 CC1 CC2 CC3 CC4 CC5 CC6 CC7 CC8

8MHz — 30 ½LS393; 30 ½LS393; 33 ½LS73; +5V

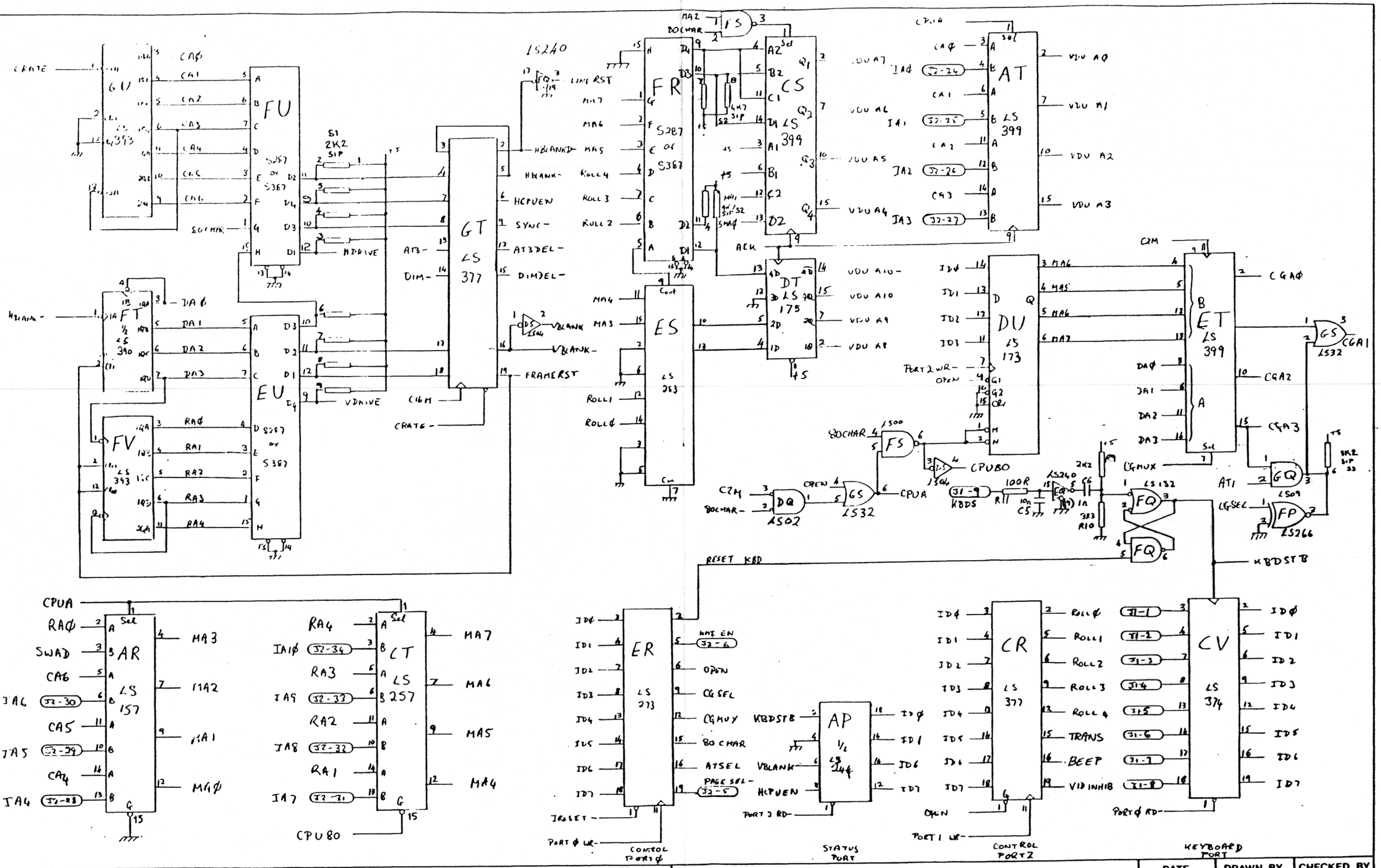
RC0 RC1 RC2 RC3 RC4 RC5 RC6 RC7 RC8 — 32 LS190 RA RB; 37 ½LS393; 37 ½LS393

ASTEC MODULATOR UM1111E36 — C16 100µ 25V; CABLE; UHF OUTPUT

COLUMN COUNTER

ROW COUNTER

18-12-79	CBL-A	380Z: VDU-2
2	13-2-80	VIDEO GENERATION
5	10-08-81	D12690 sht 2 of 2
		© 1977, 1979 DRAWING 2
		RESEARCH MACHINES LTD



MODIFICATION									
A	22/2/80								
B	23/7/80								
C	1/8/80								
D	12/9/80								
E	14/5/81	(2)							
F	31/7/81	AW							
G	11/8/81	AW							
H	26/10/81	AW							
I	10/08/84								

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
22-2-80	TB Hall	

TITLE: 80/40 VDU TIMING / PORTS

DRAWING NO D12677 sht 1 of 4

WP 1001

ATWR
VDURD
ATSEL
EP
CGSEL
MVDUEN-
OPEN
TRANS
DQ
VDUSEL-
TOPEN-
MEMWR
FS
WR40-
WR80
FT
245
240
SLEEP
HIDRIVE
VDUWR
AS
LS 374
ATϕ
AT1
AT2-
AT3-
C2M
WR80
WR40-
ISOLATE SYS RESET
BUS HOLD
(Underline)
(Dim)
(Reverse)
PORT1WR-
PORT1RD-
GQ
1K2 SIP S3
GR
LS 157
CG245EN-
CHLATCH
CGWR-
AROM
PORT2WR-
C2M
PORT1WR-
ATSEL
ATϕ
CGSEL
CHLATCH
CGA4
CGA5
CGA6
CGA7
CGA8
CGA9
CGA10
CGA11
LS273 DW
IDϕ
ID1
ID2
ID3
ID4
FD5
ID6
ID7
DV
LS 245
IRD-
MVDUEN-
VDU Aϕ
VDU A1
VDU A2
VDU A3
VDU A4
VDU A5
VDU A6
VDU A7
VDU A8
VDU A9
CW
6116
CS
OE
A10
WE
CGSEL
VDU A10-
VDU A10
ATSEL
ATWR-
GS
LS32
ATWR
ATSEL
VDURD
FQ
DR
LS 240
1K2 SIP S3
BU
CU
2114 (200nS)
EV
LS 245
CGWR-
CG245EN-
CGAϕ
CGA1
CGA2
CGA3
CGA4
CGA5
CGA6
CGA7
CGA8
CGA9
AROM
CE A10
CE A11
CGWR-
DS
LS04
FS
LS08
2516 (2532)
OE/A11
A10
VPP
EW
GW
6116
DIMG-
GV
LS 166
RAM VID
CRATE-
C16M
CI
SI
LS32

MODIFICATION		
A	23/7/80	
B	1/8/80	
C	12/8/80	
D	14/5/81	AW
E	31/7/81	AW
F	11/8/81	AW
H	26/10/81	AW
I	10/08/84	

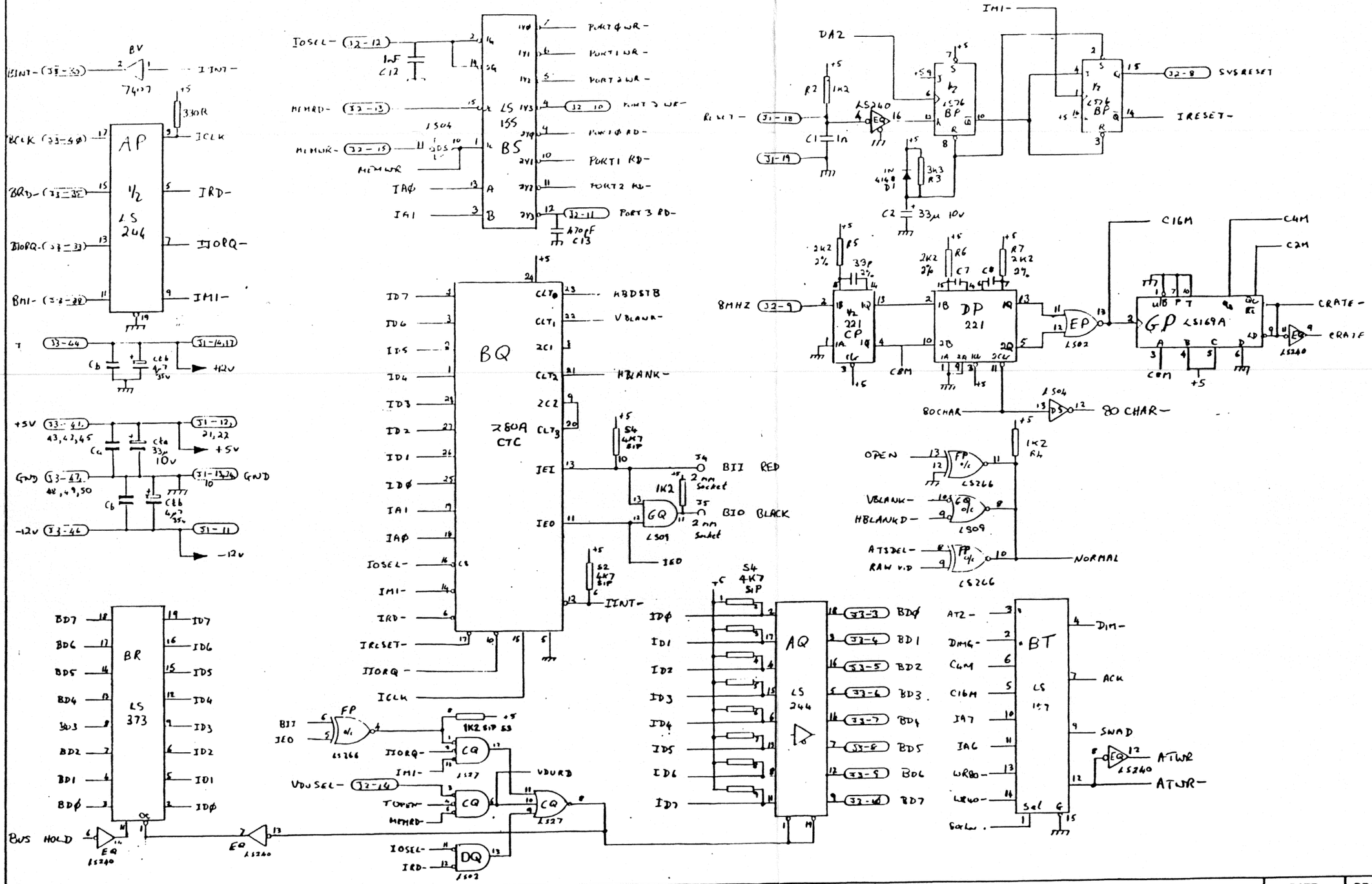
Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
23/7/80	T.Bibby	

TITLE: 80/40 VDU MEMORY

DRAWING NO. D12677
Sht 2 of 4

WP 1001



MODIFICATION		
A	14/2/80	
B	23/7/80	
C	1/8/80	
D	12/8/80	
E	19/5/81	BB
F	31/7/81	AW
G	11/8/81	AW
H	21/8/81	AW
J	10/03/84	

Research Machines Ltd

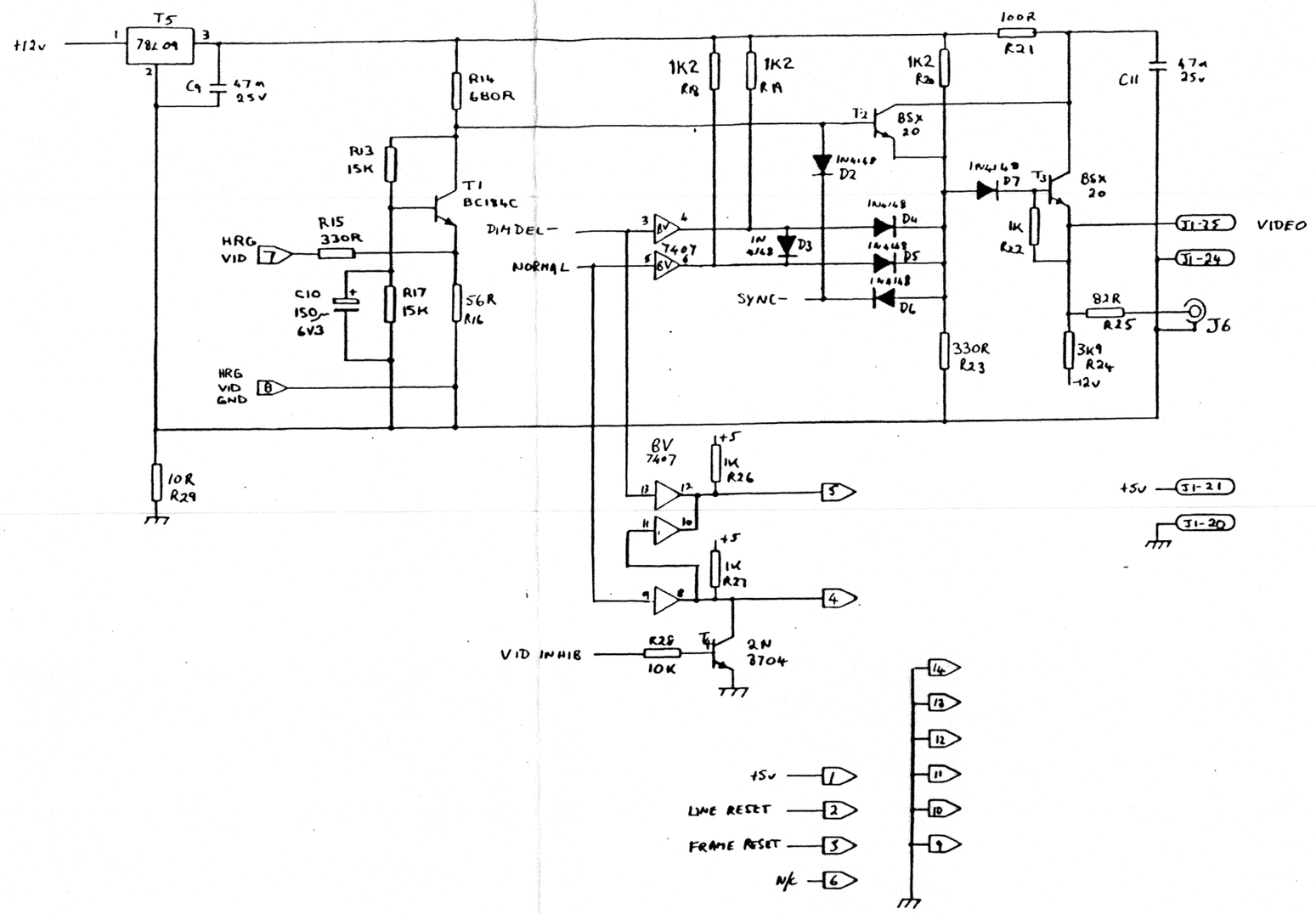
DATE	DRAWN BY	CHECKED BY
14-2-80	TB R.L-Jn.	

TITLE

80/40 VDU BUS BUFFERS

DRAWING NO. D2677
SHT 3 of 4

WP 1001



NOTES

1. ⇨ INDICATES CONNECTION TO 16-WAY DIL SOCKET AY/J7
2. T1 BC184C MIN. GAIN 500

MODIFICATION								
A	20/4/80							
B	15/5/81							
C	31/7/81	AW						
D	31/7/81	AW						
E	20/8/81	AW						
H	26/10/81	AW						
I	10/08/84							

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
20/4/80	T.B.Rhodes	

TITLE: 80/40 VDU OUTPUT

DRAWING NO. D12677 sht 4 of 4

WP 1001

BUS BUFFERING

I/O PORT DECODING

LINKS ARE SHOWN AS THE BOARD TRACKS WHICH ARE NORMALLY FOR THE MDS OPTION.

BOARD ADDRESS

MDS: LINKS UNCUT
= I/O PORTS CO HEX

FDS: CUT LID A-A16
LINK: BQ5-A016
BR4-BR5
= I/O PORTS E0 HEX

BA7 (J3-14) BA6 (J3-13) BA5 (J3-16) BA4 (J3-15) BA3 (J3-14) BA2 (J3-12) BA1 (J3-12) BAØ (J3-11)

AQ LS244 — IA7 IA6 IA5 IA4 IA3 IA2 IA1 IAØ

BQ

BR LS138

IORD- IOWR- IIORQ-

BP BP BP

IORD IOWR

CTCEN- 825IEN- 1771EN-

PORTØ WR-

IOEN-

SIP1 4K7 Vcc

BD7 (J3-10) BD6 (J3-9) BD5 (J3-8) BD4 (J3-7) BD3 (J3-6) BD2 (J3-5) BD1 (J3-4) BDØ (J3-3)

AR LS245

ID7 ID6 ID5 ID4 ID3 ID2 ID1 IDØ

BS LS273

DINT- SET DRIVE ENABLE-

MSEL SSEL DS4 DS3 DS2 DS1

BINT (J3-30)

CP CP CP

IRD- IOEN- IM1- INT-

IIORQ-

JRESET-

BM1 (J3-28) BRD (J3-35) BWR (J3-34) BIORQ (J3-33) BCLK (J3-40) BRESET (J3-1)

AP LS244

IM1- IRD- IWR- IIORQ- ICLK1 IRESET- ICLK2

Vcc 5mm A

ICLK1

BU ½ LS393 — 2MHz 1MHz 4µs

BU ½ LS393 — T5 T4 T5 6 — 64µs

DP 4020 — Q5 Q14 Q10 — 2ms 64ms

J3-44 +12v

J3-41,43 (+5v) Vcc

J3-45,47 J3-48,50 0v

J1-46 -12v

Q1 79L05 — -5v

22µ 22µ

6-12-79	380Z: FLOPPY DISC CONTROLLER AND SIO4	
2	(ALSO SIO1A / LPO4)	
1 17-12-79	© 1978,1979	DRAWING NO FDC1
3 25-1	RESEARCH MACHINES LTD	

+5v

ID7 ID6 ID5 ID4 ID3 ID2 ID1 IDØ IA1 IAØ CTCEN- IRESET- IRD- IIORQ- IM1- ICLK2

Z80A-CTC

DQ

ZCT0 TRG0 ZCT1 TRG1 ZCT2 TRG2 TRG3

ES LS74 — DRIVE ENABLE — SET DRIVE ENABLE-

CQ — SIP2 — 64ms

ES LS74 — HLT — HLD-

CQ CQ — CR — HLD IN — 2ms

HMCC — ECUT — 2MHz 4µs

64ms (NOT USED)

R14 330R — ICLK2

SIP2

C4 1000p — R12 12K

½ LS123 DU — >1.5µs

INT-

CR

SERIAL INTERFACE

J1-9 -12v J1-6 Vcc

8251 ER

ID7 ID6 ID5 ID4 ID3 ID2 ID1 IDØ IAØ C/D CS RD WR RESET CLK

825IEN- IORD- IOWR- IRESET- 2.111Hz

CP LINK3

TxC RxC TxD RxD DTR DSR RTS CTS

75188 AV — J1-1

75189 BV — C1 470p — J1-3

J1-4

AV — J1-7

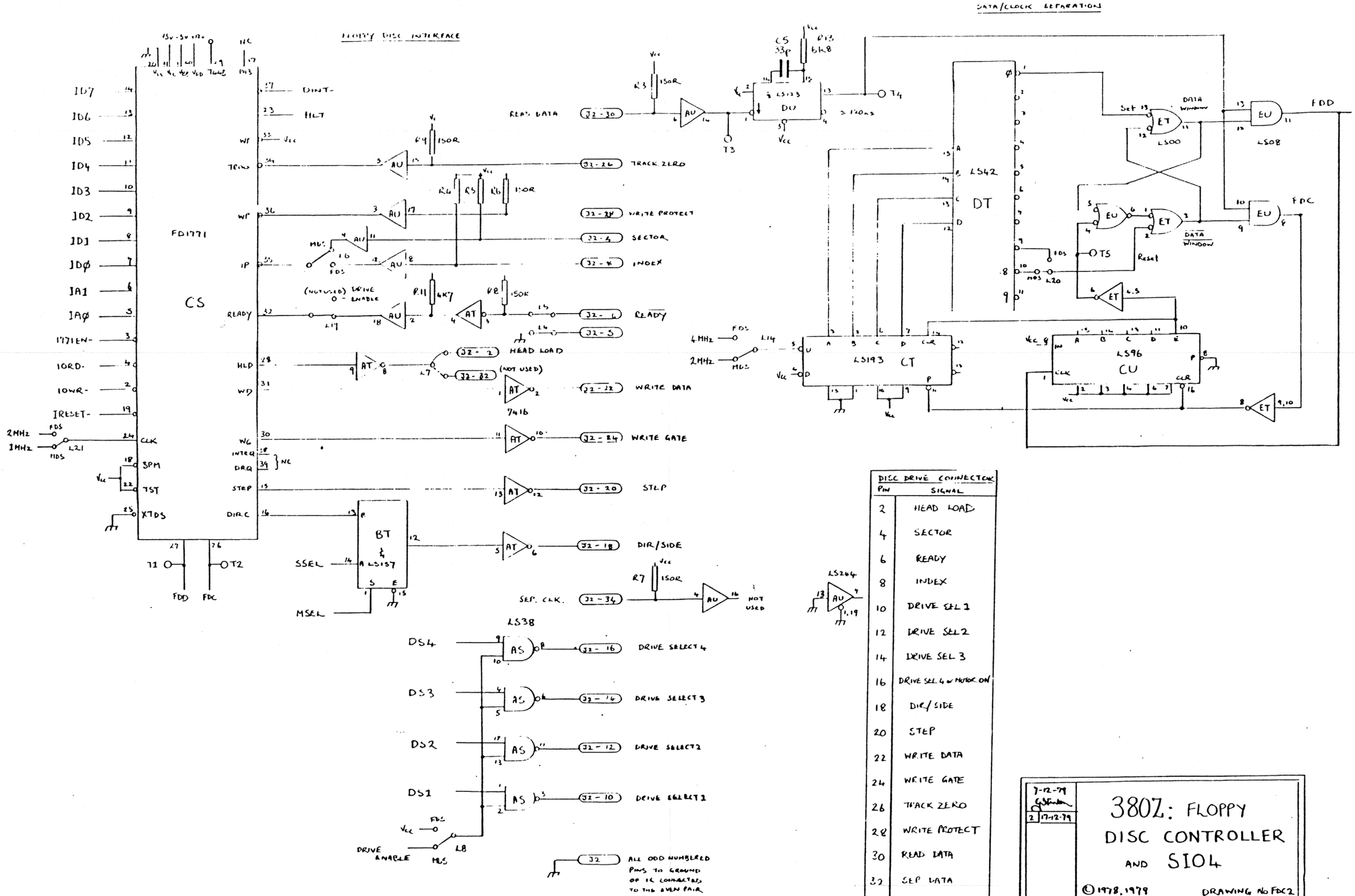
R1 4K7 — BV — C3 470p — J1-5

AV — J1-8

R10 4K7 — BV — C2 470p — J1-10

2R2 R2 — J1-2

+5v


FLOPPY DISC INTERFACE
FD1771
CS
ID7
ID6
ID5
ID4
ID3
ID2
ID1
IDØ
IA1
IAØ
1771EN-
IORD-
IOWR-
IRESET-
2MHz
1MHz
FDS
MDS
L21
CLK
SPM
TST
XTDS
DINT-
HLT
WF
TRØ0
WP
IP
READY
HLD
WD
WG
INTRQ
DRQ
STEP
DIRC
NC
T1
T2
FDD
FDC
READ DATA
TRACK ZERO
WRITE PROTECT
SECTOR
INDEX
READY
HEAD LOAD
WRITE DATA
WRITE GATE
STEP
DIR/SIDE
SSEL
MSEL
BT
LS157
SEP. CLK.
NOT USED
(NOT USED) DRIVE 0 - ENABLE
LS38
DS4
DS3
DS2
DS1
DRIVE SELECT 4
DRIVE SELECT 3
DRIVE SELECT 2
DRIVE SELECT 1
DRIVE ENABLE
L8
ALL ODD NUMBERED PINS TO GROUND OF IC CONNECTED TO THE EVEN PAIR
DATA/CLOCK SEPARATION
LS123
DU
≥ 120ns
LS42
DT
LS193
CT
LS96
CU
LS00
LS08
LS20
T3
T4
T5
Reset
DATA WINDOW
4MHz
2MHz
DISC DRIVE CONNECTOR
PIN SIGNAL
2 HEAD LOAD
4 SECTOR
6 READY
8 INDEX
10 DRIVE SEL 1
12 DRIVE SEL 2
14 DRIVE SEL 3
16 DRIVE SEL 4 or MOTOR ON
18 DIR/SIDE
20 STEP
22 WRITE DATA
24 WRITE GATE
26 TRACK ZERO
28 WRITE PROTECT
30 READ DATA
32 SEP DATA
34 SEP CLOCK
7-12-79
2 17-12-79
380Z: FLOPPY DISC CONTROLLER AND SIO4
©1978,1979
DRAWING NO FDC2
RESEARCH MACHINES LTD

MDS & 480Z VERSIONS: 380Z : 480Z } 8MHz
LATER (ie WITH PRE-COMPENSATION ON MDS & 480Z VERSION)
380Z MDS: MDS 2K : MDS 8K : 480Z } PHI.
380Z FDS: FDS 2K : FDS 8K } 8MHz.
ISSUE 5
380Z 2K, 380Z 8K, 480Z } XCLK.

SEE ECN160 FOR FULL DETAILS OF EARLY & LATER

BRESET- J3-1 → IRESET-
BAΦ J3-11 → IAΦ (LK13 1–2)
BA12 J3-23 → TA12
BA13 J3-24 → TA13
BRD- J3-35 → IRD-
BMREQ- J3-36 → IMREQ-
BM1- J3-38 → M1- → IM1- (LK13 23–24)
BCLOCK J3-40 → ICLOCK
IC5 74ALS1244

BAΦ J3-3 … BD7 J3-10 → IC4 74LS245 → IDΦ … ID7

IC9 74ALS574 (D Q): IDΦ … ID7 → DΦ … D7; HWR-, DRD-
IC18 74ALS574 (D Q): DΦ … D7 → IDΦ … ID7; DWR-, HRD-

IC27 74ALS1244: MOTOR, DTIMED, DRDWT-, DWRWT- → DSTRD-
IC27 74ALS1244: INUSE, HTIMED, HRDWT-, HWRWT- → HSTRD-

IC12 74ALS576 (D Q): IWD-, DWD-, WD, LATE, DWR-, HWR-, DSTRD-, HSTRD- → IWD, 2DWD, DWD-, DLATE-, DDW, DHW, DDST, DHST

BA9 J3-20 … BPAGE- J3-2 → IC10 74ALS1244 → IA9, IA1 … IA6 (LK13 3–4 … 13–14)

IIORQ-, IWR-, IRD- (LK13 IORQ- 22–21, WR- 18–17, RD- 20–19)

380Z I/O MAP DECODE — IC19 PAL-1216-2
IA1 … IA7, BIEI → BDIR-, CTCEN-, SIOEN-, HSTRD-, HRD-, HWR-, BIEO

RN2-9 4K7, RN2-8 4K7 → Vcc

BA8 J3-19, BWR- J3-34, A10 J3-21, BA11 J3-22, BIORQ- J3-33, BA7 J3-18, BA14 J3-25, BA15 J3-26 → IC11 74ALS1244 → IA8, IWR-, IIORQ-, IA7 (LK13 15–16), IA14, IA15

IC Nº	DEVICE
13/14	74LS00
20	74LS74
22	74LS32N
23	74LS107
30	74LS123

RESET-, DRD-, Vcc → IC20 PR/D/CL → DRDWT-
HWR-, DRDWT- → IC22 → HWTΦ-
HWTΦ-, HWR- → IC13 → CLDRD-
HRDWT-, HRD- → IC22 → HWT1-
HWR-, DHW, CLDRD- → IC13 → HWT1-
HWTΦ-, HWT1- → IC13 → HWAIT

HWAIT, Vcc, R19 100K, C39 10n, IC30 250µs → HLONG-, HLONG
HLONG, HSTRD- → IC14 → HSTIME-
RESET-, HSTIME-, DHST → IC23 → HTIMED-, HTIMED
HTIMED- → IC30 CL

RESET-, HRD-, Vcc → IC20 PR/D/CL → HRDWT-
DWR-, DDW → IC13 → CLHRD-
DWR-, HRDWT- → IC22 → DWTΦ-
DRDWT-, DRD- → IC22 → DWT1-
DWTΦ-, DWT1- → IC13 → DWAIT

DWAIT, Vcc, R12 220K, C32 33µ, IC30 10s → DLONG-, DLONG
DLONG, DSTRD- → IC14 → DSTIME-
RESET-, DSTIME-, DDST → IC23 → DTIMED, DTIMED-
DTIMED- → IC30 CL

ECN	Date	Iss
1	23.2.84	A
208	01-05-84	1

UNLESS OTHERWISE STATED ASSUME:-
ANGULAR TOLERANCE ± 1/2°
WHOLE UNITS ± 0,6mm
1 DECIMAL PLACE ± 0,1mm
GEOMETRICAL TOLERANCES SEE BS308 METRIC
THIRD ANGLE PROJECTION

RESEARCH MACHINES
RESEARCH MACHINES LTD, Mill St, Oxford, OX2 0BW.

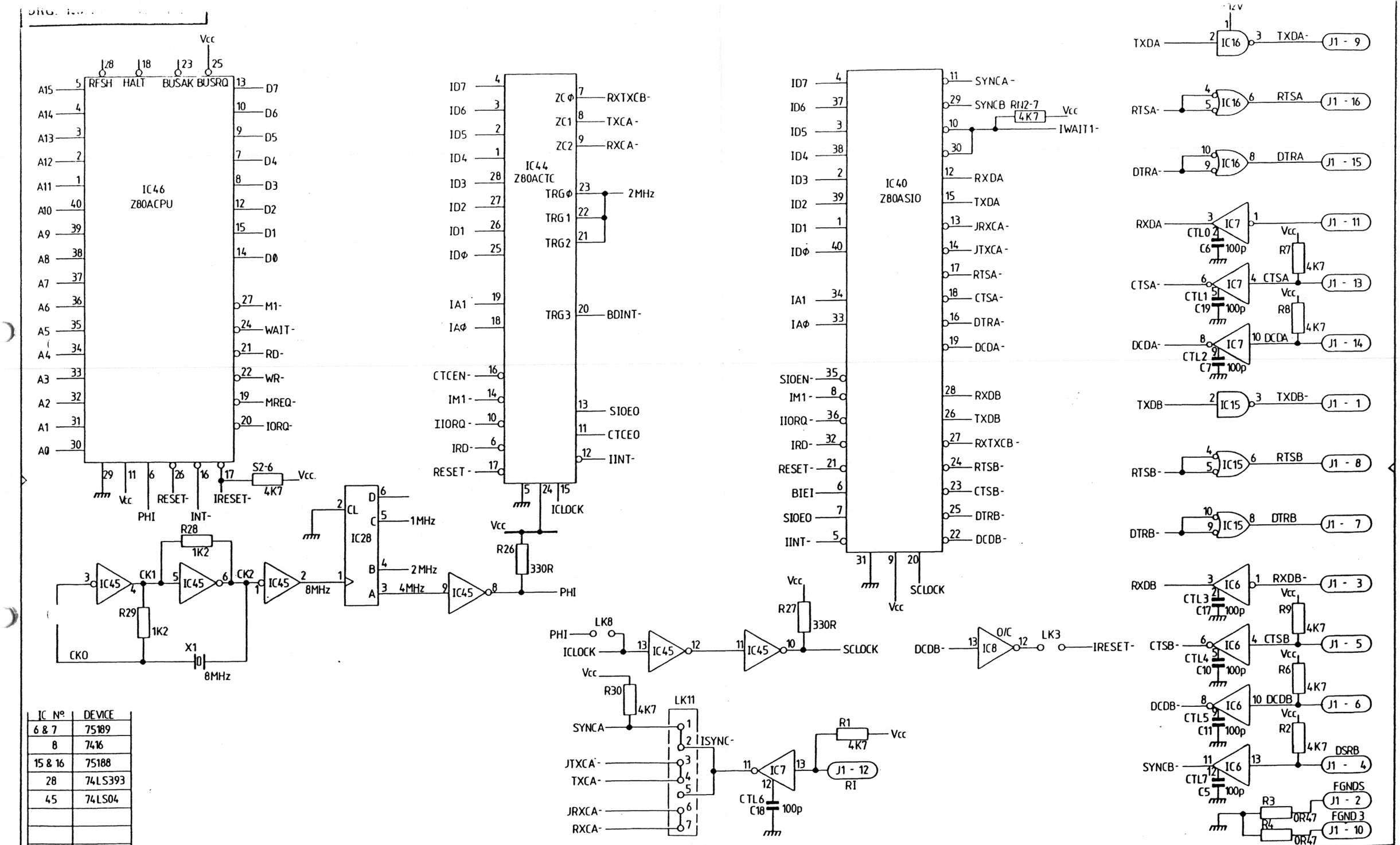
TITLE: CIRCUIT DIAGRAM IDC 380Z (BUS INTERFACE DECODE)

SCALE :

DRN. RB
DATE 22-2-84
APRD. Garth Davies
CHKD.

DRG. No. D12559 Sht 1 of 4

© RESEARCH MACHINES LTD.



IC Nº	DEVICE
6 & 7	75189
8	7416
15 & 16	75188
28	74LS393
45	74LS04

E.C.N.	Date	
1	23-2-84	208
A	01-05-84	—

UNLESS OTHERWISE STATED ASSUME :-
ANGULAR TOLERANCE ± 1/2°
WHOLE UNITS ± 0,5mm
1 DECIMAL PLACE ± 0,1mm
GEOMETRICAL TOLERANCES SEE BS308 METRIC
THIRD ANGLE PROJECTION

RESEARCH MACHINES

RESEARCH MACHINES LTD, Mill St. Oxford, OX2 0BW.

TITLE :
CIRCUIT DIAGRAM IDC 380Z
(CPU, SERIAL INTERFACE & CLOCKS)

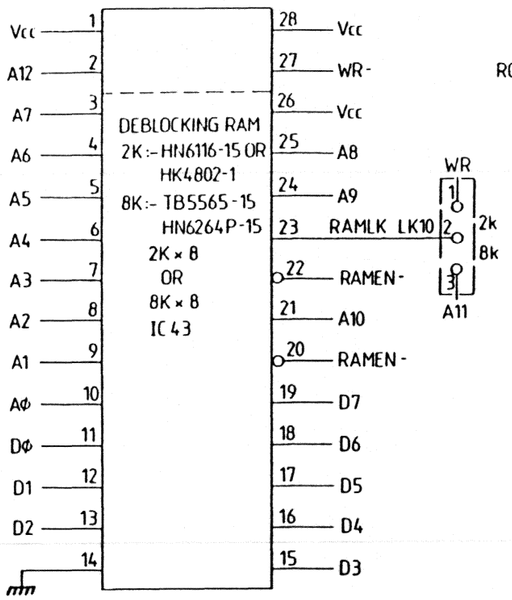
SCALE :

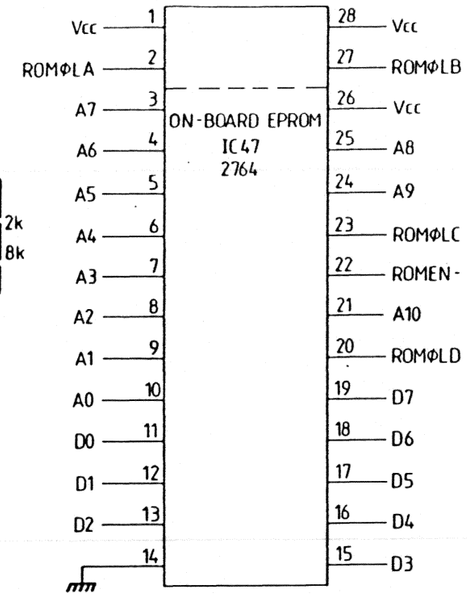
DRN. RB
DATE 22-2-84
APRD
CHKD.

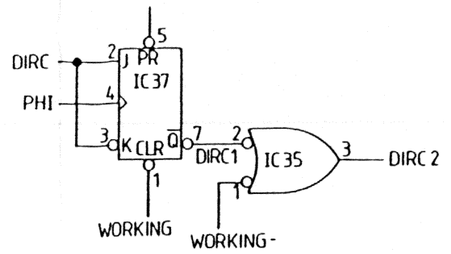
DRG. No. D12559 Sht 2 of 4.

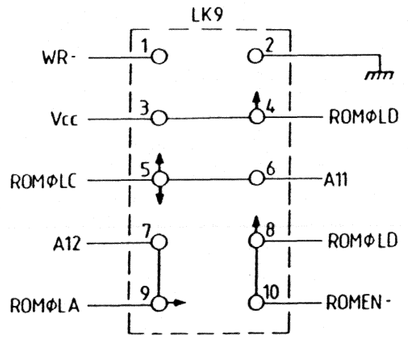
© RESEARCH MACHINES LTD.

LK10 LINK PINS 1&2 FOR 2K,
PINS 2&3 FOR 8K



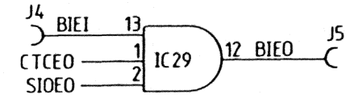


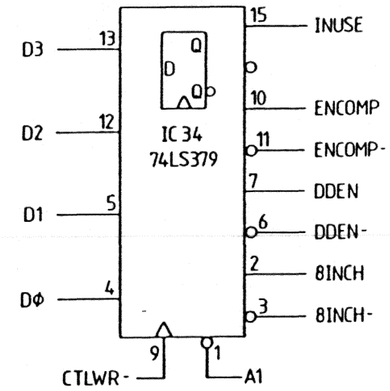


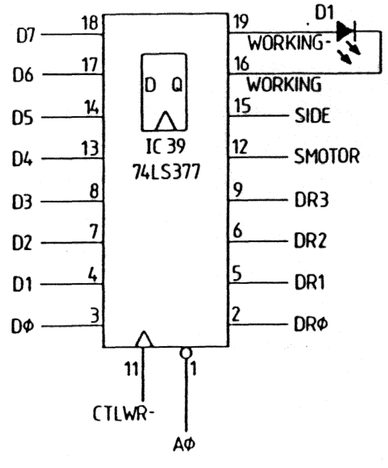


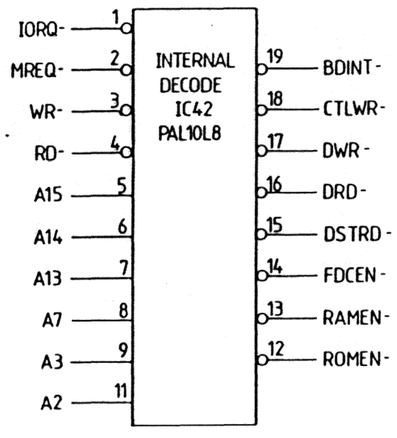
ROM SELECT LINKS LK9
PRE-LINK FOR 2764 OR
LINK FOR DEVICES AS
SHOWN

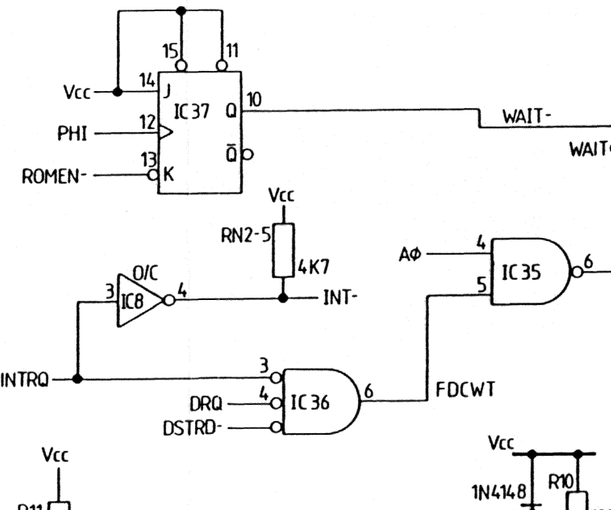
Pin	to	Pin	DEVICE
2	..	4	2564
3	-	5	2516/2532/2716
5	-	6	2732
5	-	7	2564
6	..	8	2532/2564
8	..	10	2716/2516/2732
9		10	2564











IC No.	DEVICE
1	7407
2	74LS244
8	7416
29	74LS11
35	74LS00
36	74LS27
37	74LS109

Iss.	Date	E.C.N.
A	23-2-84	1
	01-05-84	208

UNLESS OTHERWISE STATED ASSUME:-
ANGULAR TOLERANCE ± 1/2°
WHOLE UNITS ± 0,5mm
1 DECIMAL PLACE ± 0,1mm
GEOMETRICAL TOLERANCES SEE BS308 METRIC
THIRD ANGLE PROJECTION

RESEARCH MACHINES

RESEARCH MACHINES LTD, Mill St, Oxford, OX2 0BW.

TITLE:
CIRCUIT DIAGRAM IDC 380Z
MEMORY, WAIT STATE & INTERNAL DECODE

SCALE :

DRN. RB
DATE 22-2-84
APRD. Keith M Davis
CHKD.

DRG. No. D12559 Sht 3 of 4

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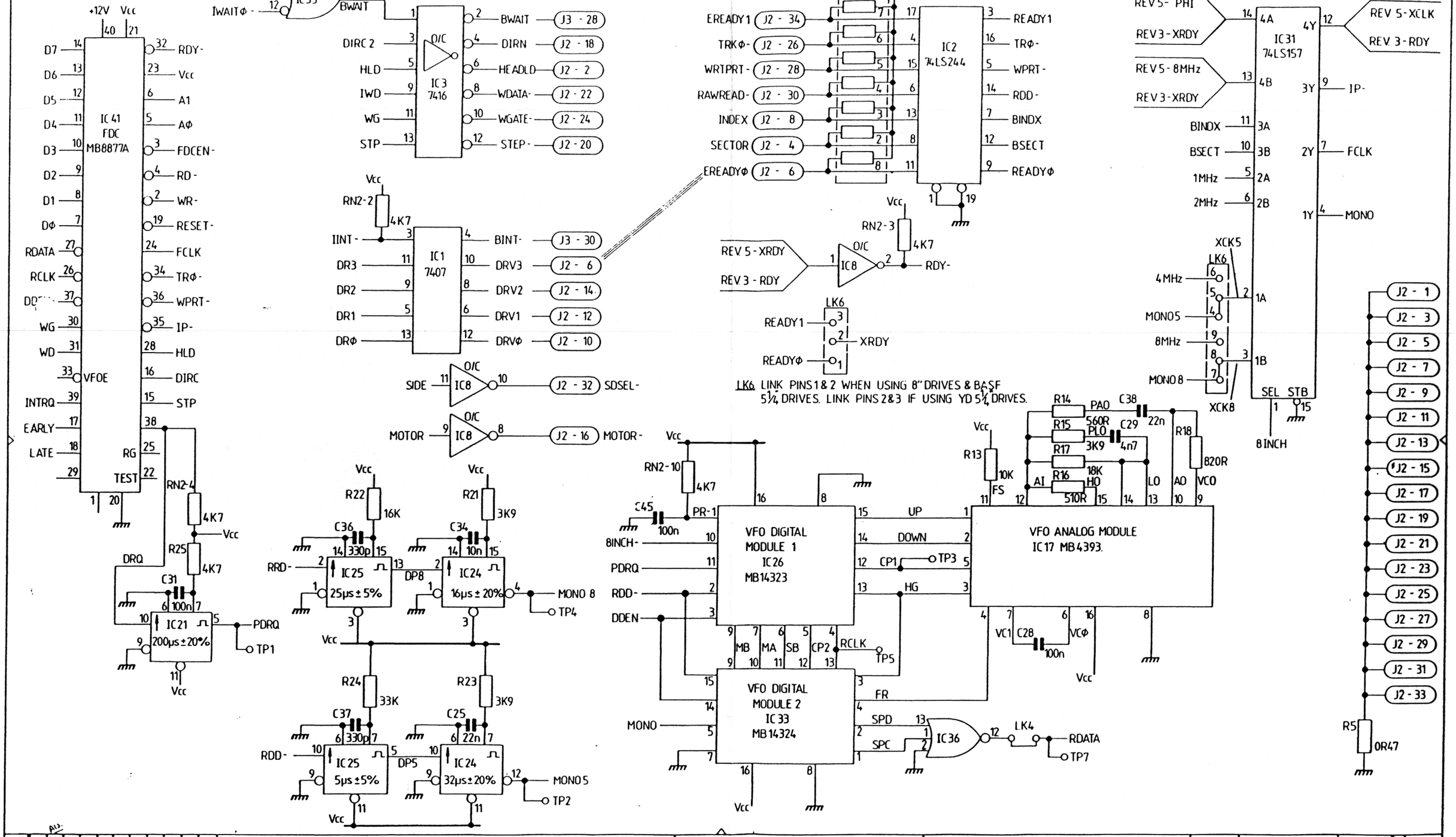

IC Nº	DEVICES
8	7416
21,24,25	74LS123
36	74LS27

E.C.N. 1 208 AU
Date 23-2-84 21-SEP-84
1 A

UNLESS OTHERWISE STATED ASSUME :-
ANGULAR TOLERANCE ± 1/2°
WHOLE UNITS ± 0.5mm
1 DECIMAL PLACE ± 0.1mm
GEOMETRICAL TOLERANCES SEE BS308 METRIC
THIRD ANGLE PROJECTION

RESEARCH MACHINES

RESEARCH MACHINES LTD. Mill St. Oxford. OX2 0BW.

TITLE :
CIRCUIT DIAGRAM IDC 380Z
(DISK DRIVE INTERFACE)

SCALE :

DRN. RB
APRD.
DATE 22-2-84
CHKD.

DRG. No. D12559 Sht 4 of 4.

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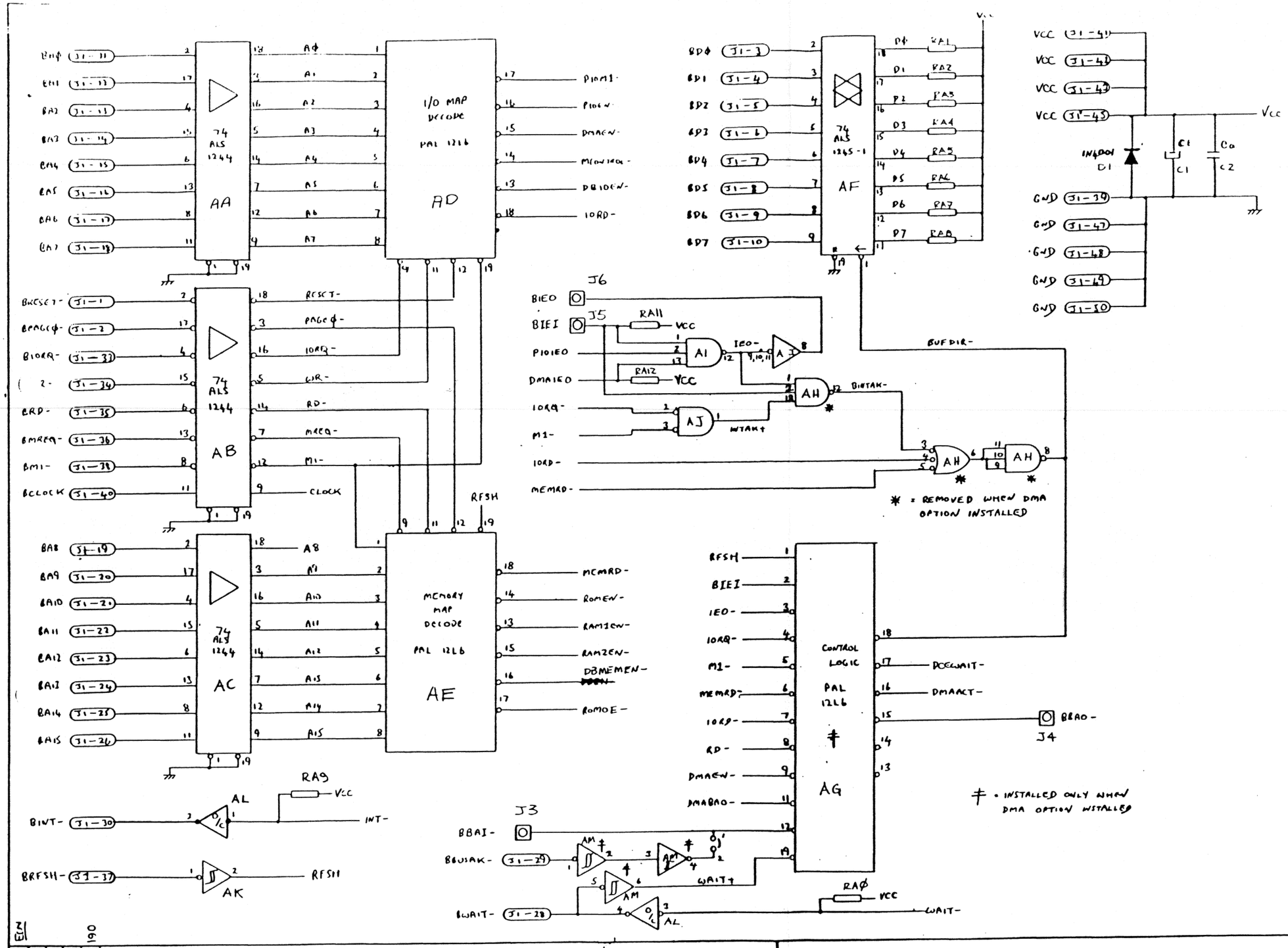


MODIFICATION			
A	FAF	21/7/82	
B	LAF	17-2-82	
C	LAF	17-2-82	
1	DJL	2-2-82	

EIN 190

WP 1001

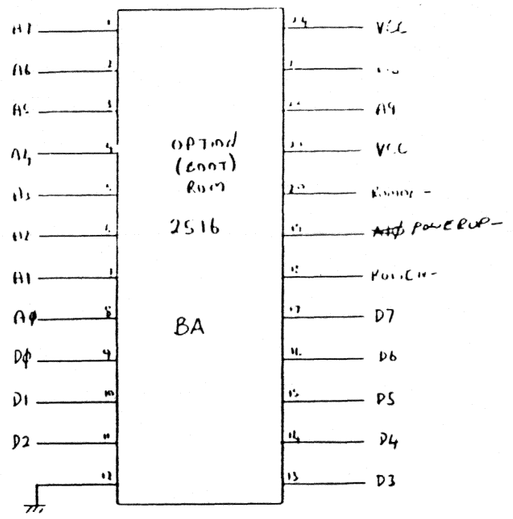
Research Machines Ltd

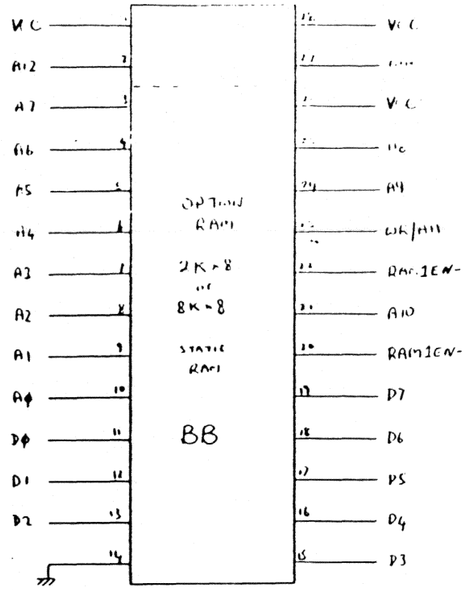
DATE	DRAWN BY	CHECKED BY
15/7/82	K. Ford	

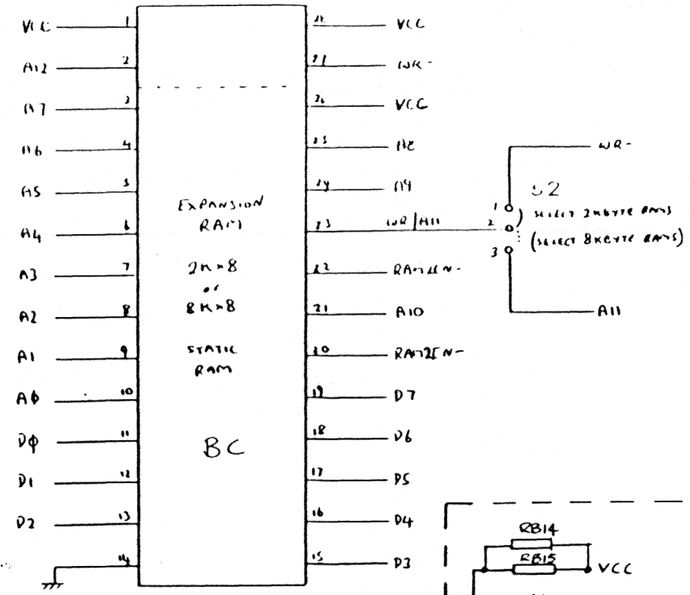
TITLE: HIB Issue 0/0

BUS INTERFACE AND CONTROL LOGIC

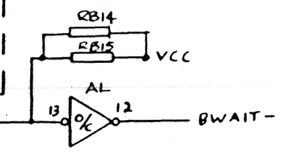
DRAWING NO. D12662 ~~HIB~~ 1/4 ~~V1.2~~

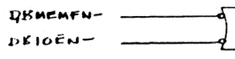


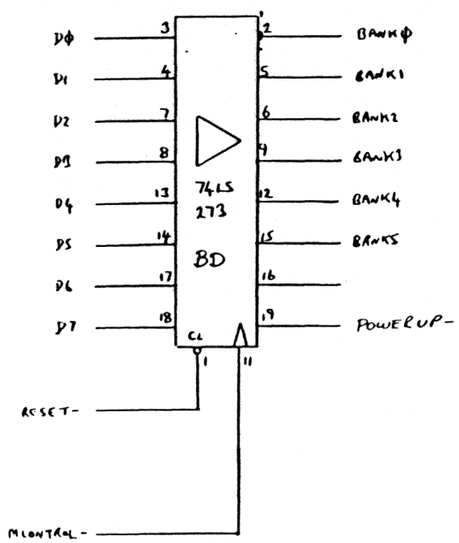


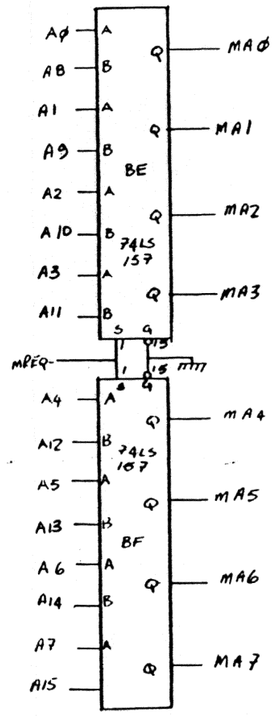


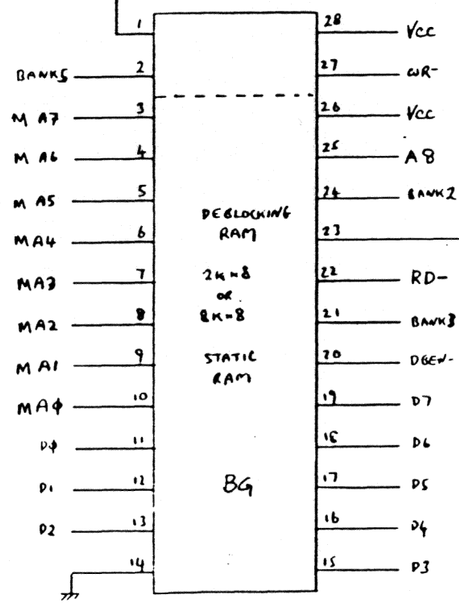
NOT FITTED

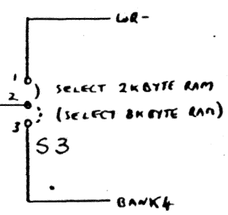












ECN	MODIFICATION	
190	A	14-7-82
	B	28-7-82
	C	[illegible]
	1	AB / 2-2-84

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
5/7/82	H FW	

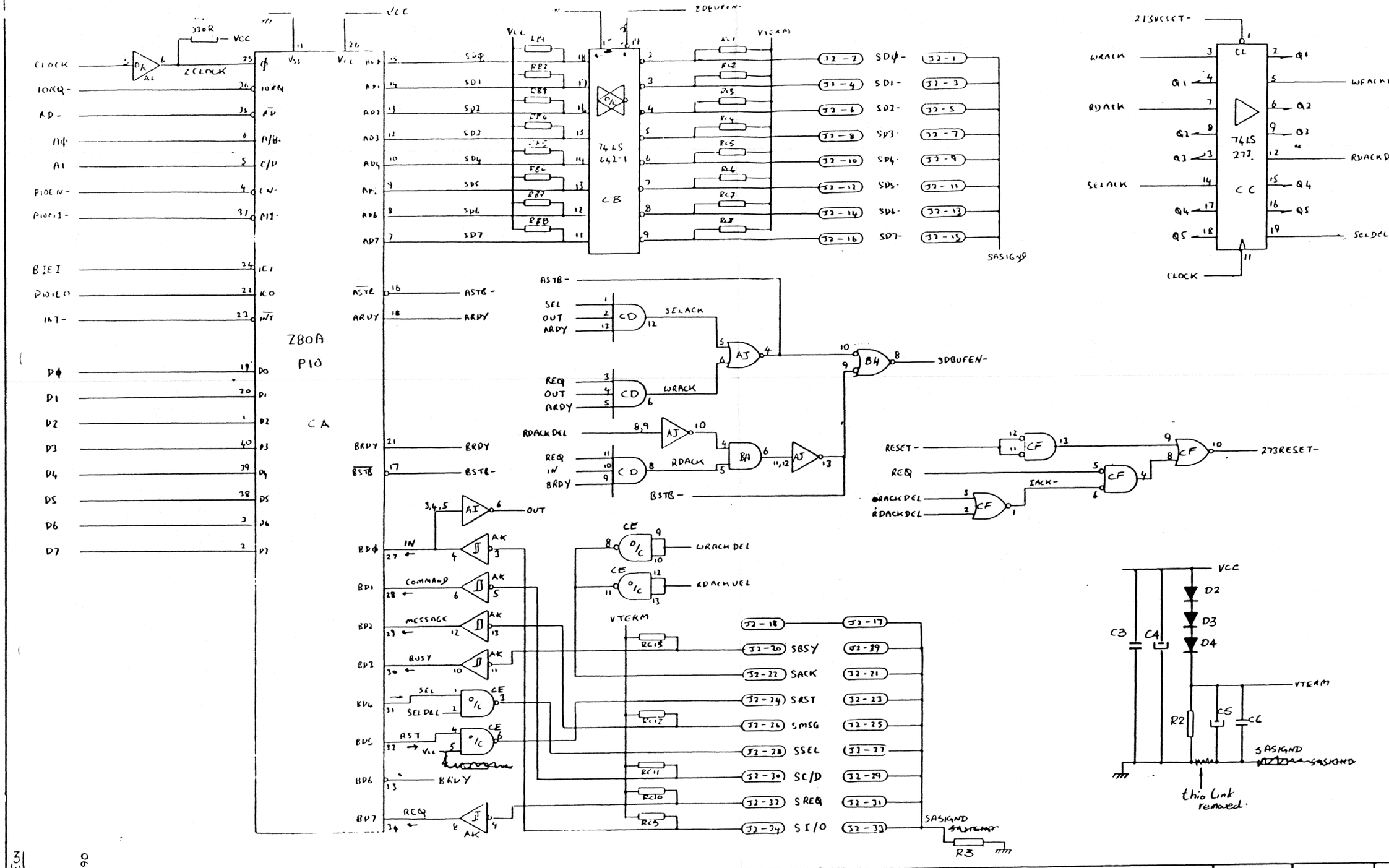
TITLE: HIB Issue Ø/0

MEMORY AND ASSOCIATED CONTROL

DRAWING NO. D12662

HIB 2/4 ~~V1.2~~

WP 1001



ECN 190

MODIFICATION		
A	14-7-82	
B	[illegible]	
C	23-7-82	
1	2-2-84	

WP 1001

Research Machines Ltd

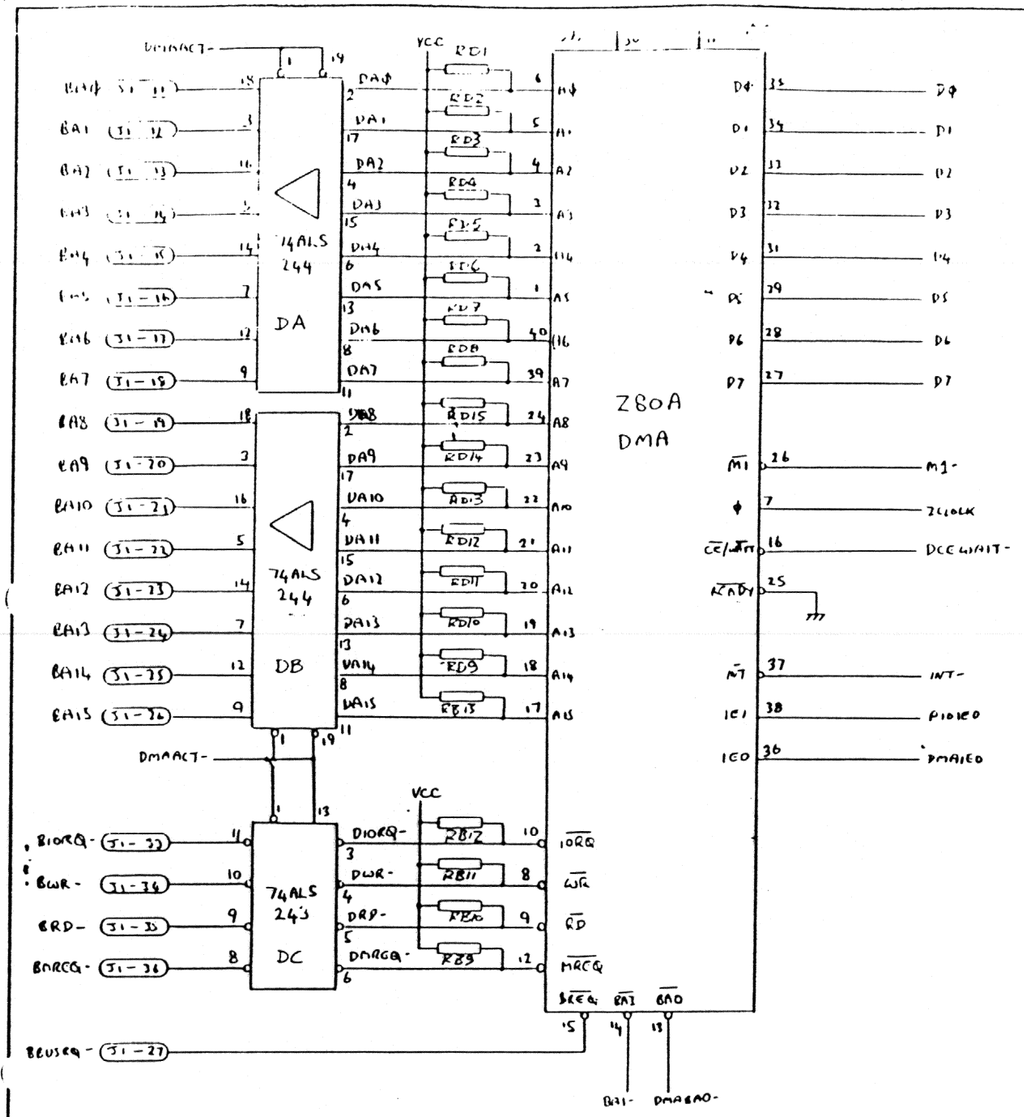
DATE	DRAWN BY	CHECKED BY
5/7/82	H [illegible]	

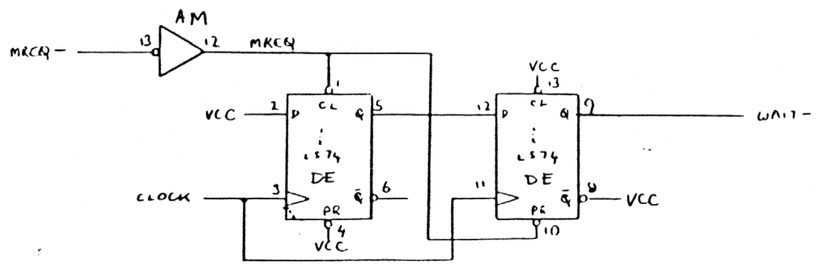
TITLE: HIB Issue Ø/Ø

P10 AND SASI INTERFACE

DRAWING NO. D12662

~~HIE~~ 3/4 ~~V1.7~~





ECN	190
MODIFICATION A	15.7.82
B	23-7-82
C	2-2-84

WP 1001

Research Machines Ltd

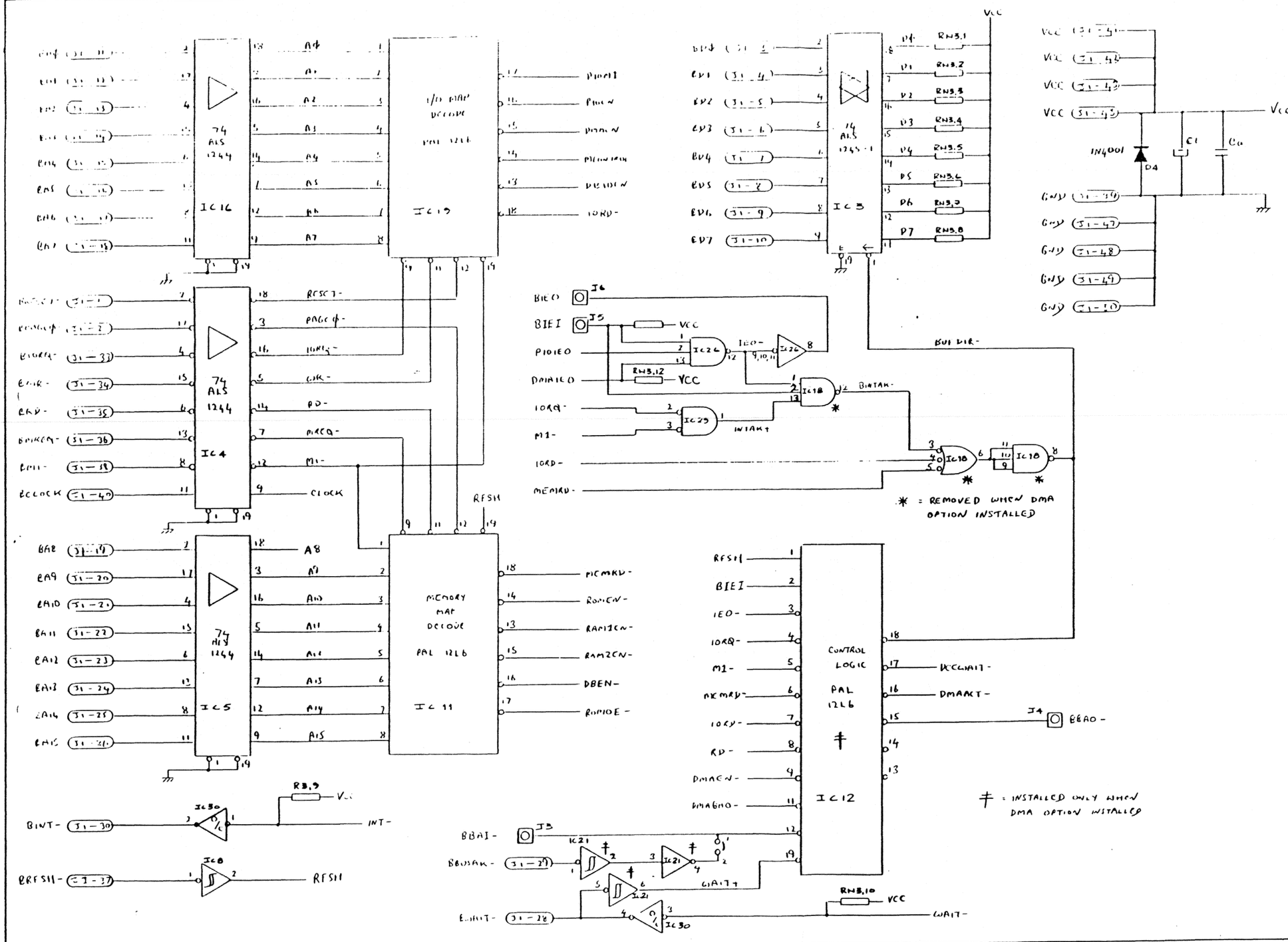
DATE	DRAWN BY	CHECKED BY
6/7/82	K Ford	

TITLE: HIB Issue ϕ/ϕ

DMA CHIP I/O SUPPORT (OPTIONAL)

DRAWING NO. D12662

~~HIB~~ 4/4 ~~V1.2~~



MODIFICATION		
A	PAF	28/7/83
B	K.R.J	23-7-83

WP 1001

Research Machines Ltd

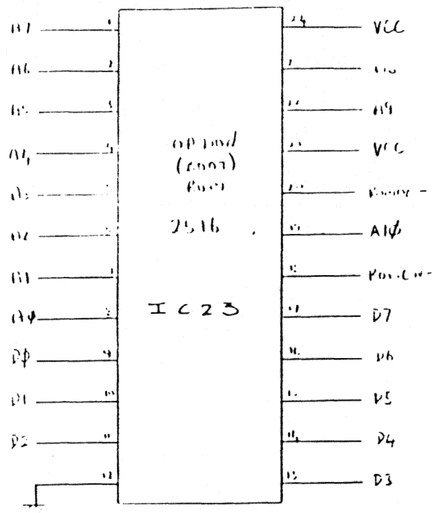
DATE	DRAWN BY	CHECKED BY
15/7/82	K Ford	

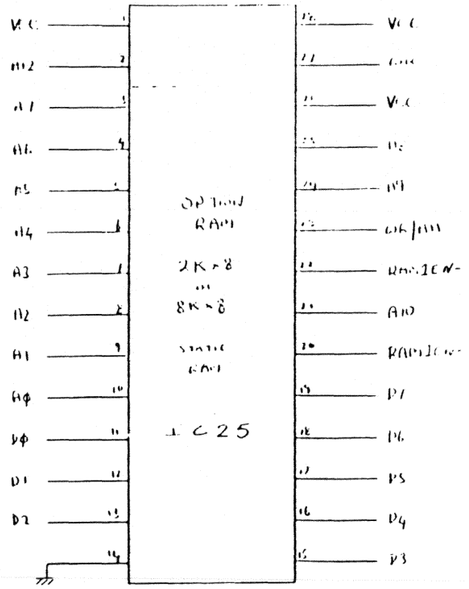
TITLE

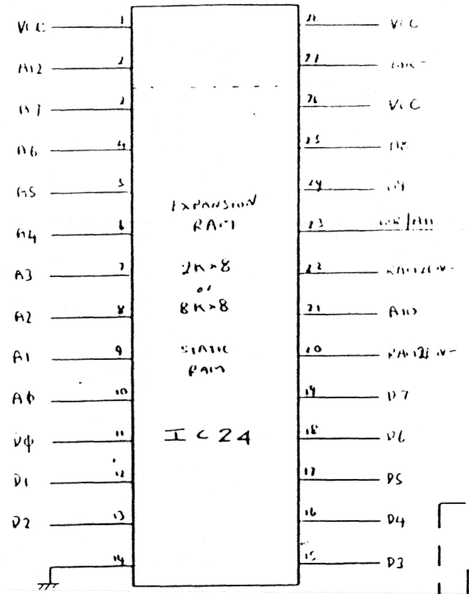
BUS INTERFACE AND CONTROL LOGIC HIB 155 2

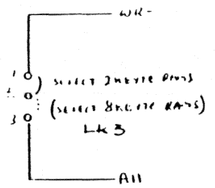
DRAWING NO.

HIB 1/4 V1.2

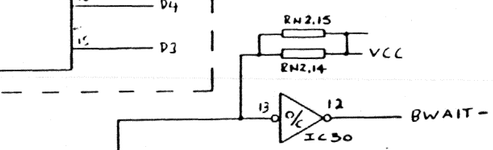


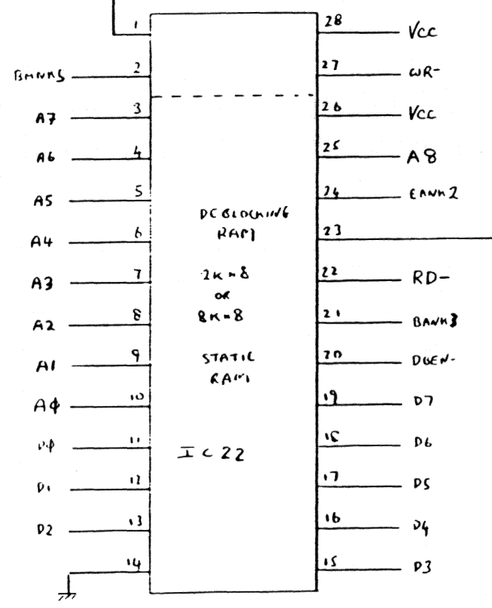


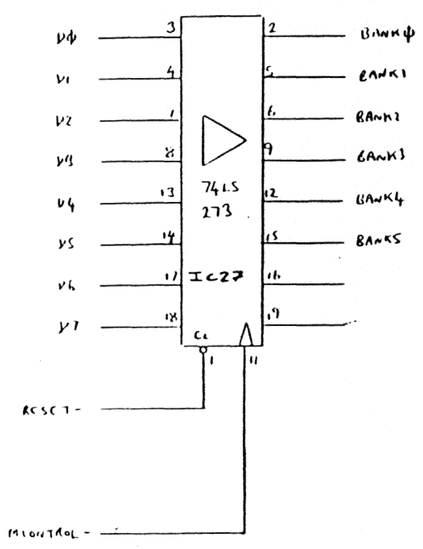




NOT FITTED







MODIFICATION			
A	[illegible]	16-7-82	
B	[illegible]	18-7-82	
C	[illegible]	22-2-83	

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
5/7/82	M Ford	

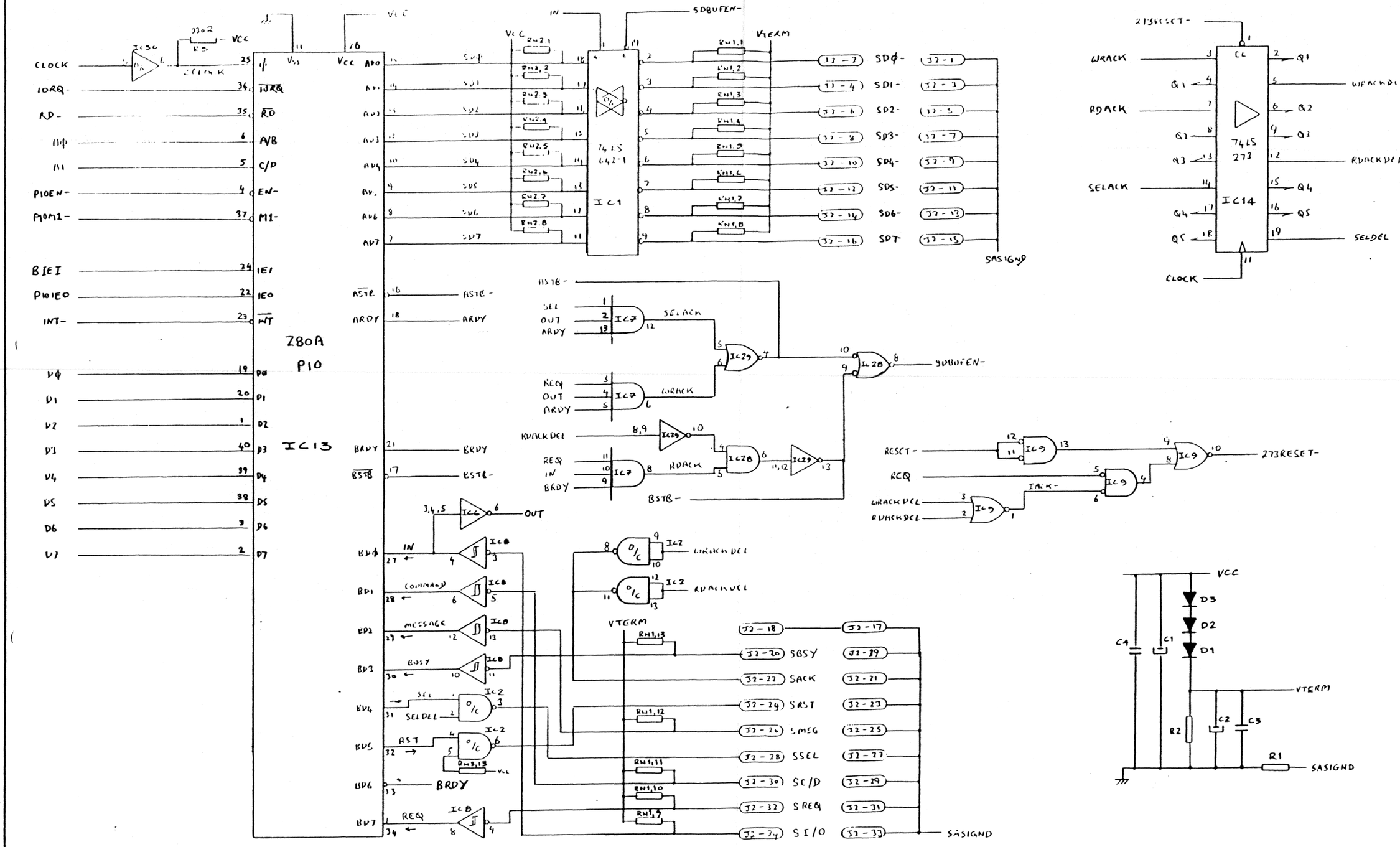
TITLE

MEMORY AND ASSOCIATED CONTROL HIB 1552

DRAWING NO.

HIB 2/4 V1.2

WP 1001



MODIFICATION		
A	[illegible]	14-7-82
B	[illegible]	[illegible]
C	[illegible]	27-7-83

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
5/7/82	H Ford	

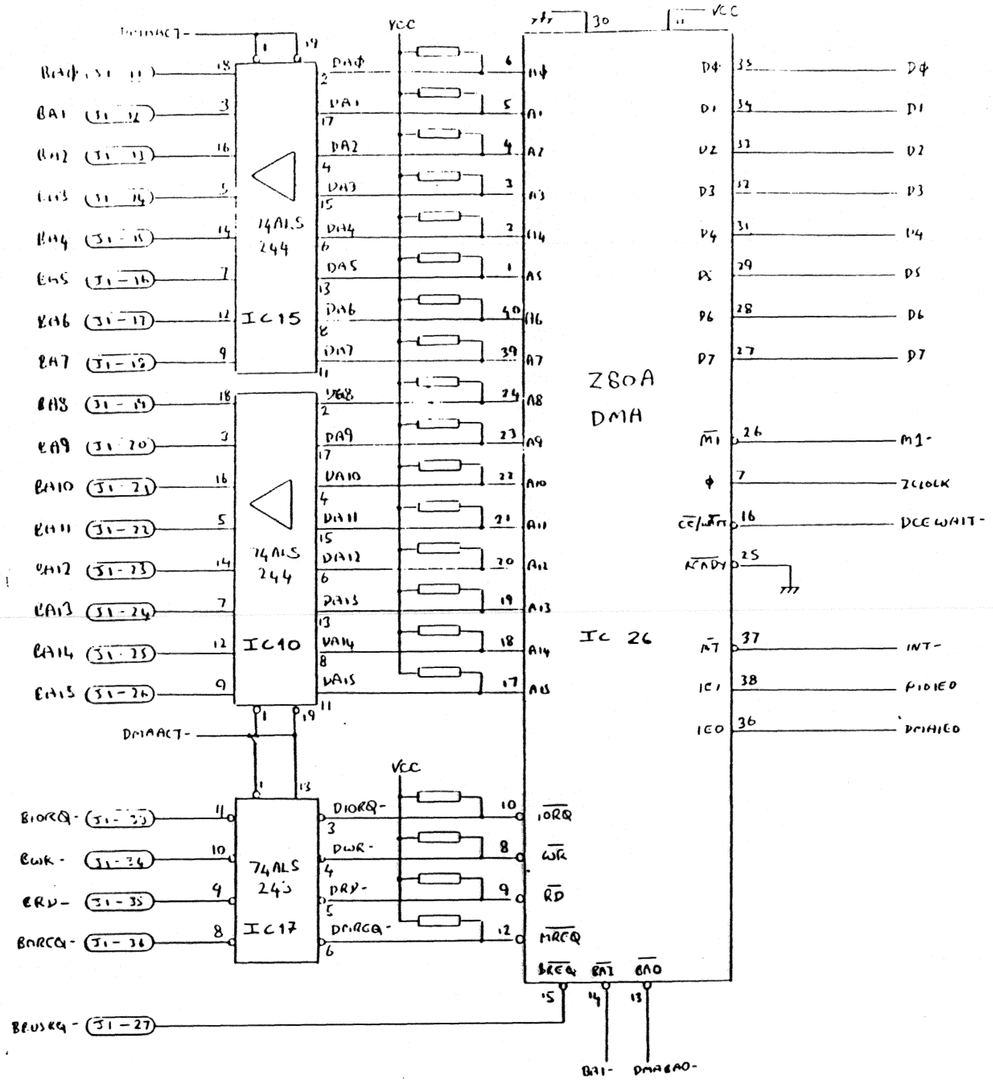
TITLE

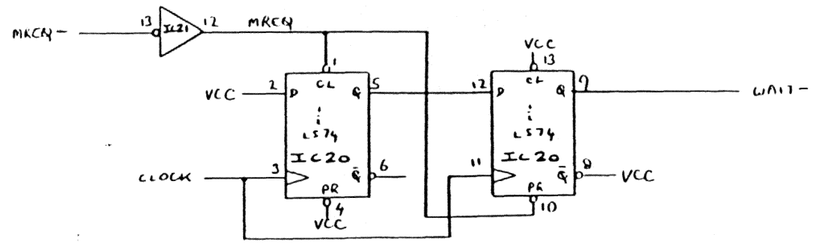
PIO AND SASI INTERFACE HIB 155 2

DRAWING NO.

111E 3/4 V1.2

WP 1001





MODIFICATION		
A	4d	15.7.82

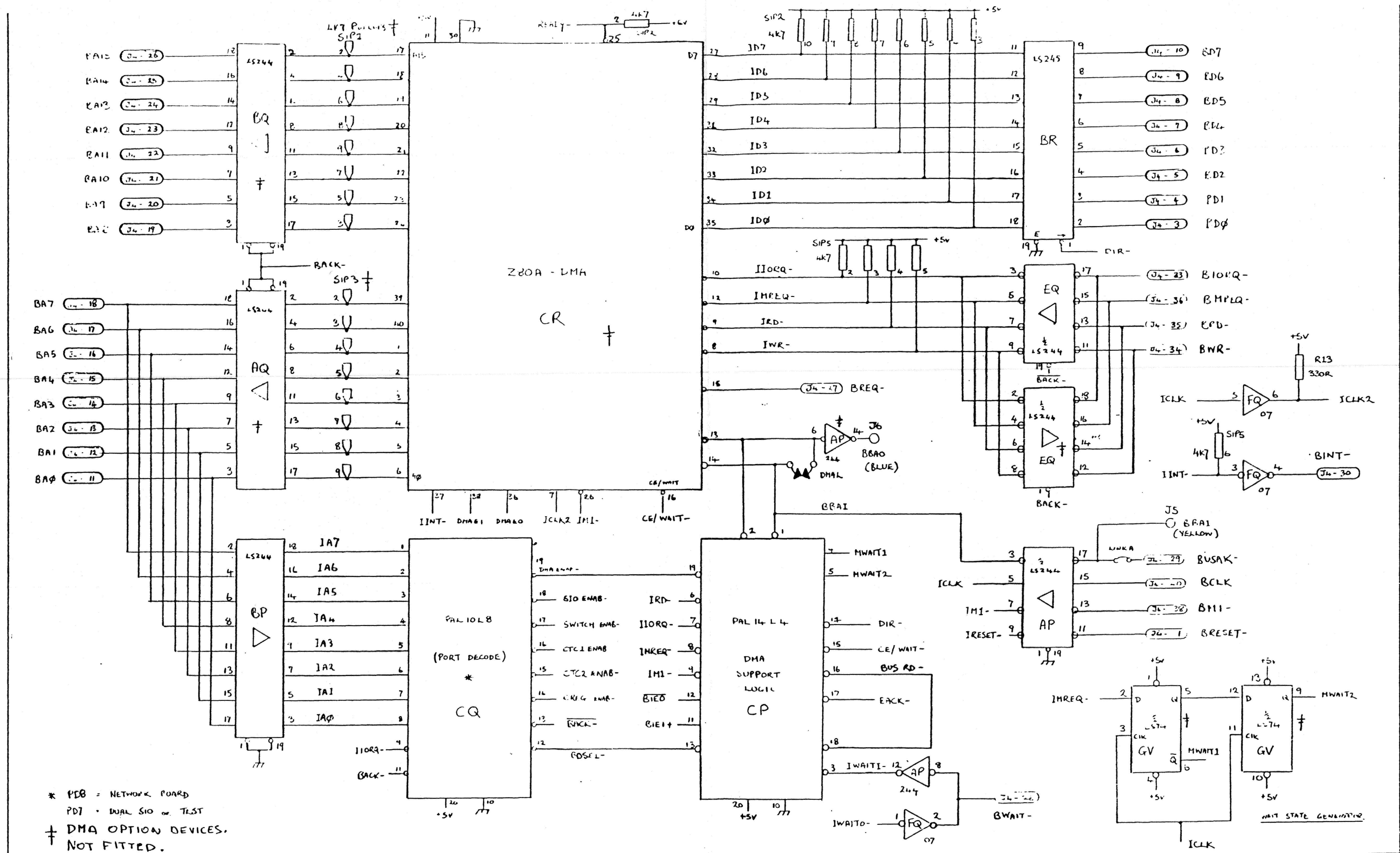
WP 1001

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
6/7/82	K Ford	

TITLE: DMA CHIP AND SUPPORT (OPTIONAL) HIB 1332.

DRAWING NO. HIB 4/4 V1.2



LS244
BQ
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BAØ
AQ
BACK-
SIP3
4K7 PULLUPS
SIP1
LS244
BP
IA7
IA6
IA5
IA4
IA3
IA2
IA1
IAØ
Z80A - DMA
CR
READY-
4K7
SIP2
+5V
ID7
ID6
ID5
ID4
ID3
ID2
ID1
IDØ
IIORQ-
IMREQ-
IRD-
IWR-
BREQ-
SIP5
4K7
AP
J6
BBAO
(BLUE)
DMAL
IINT-
DMAEI
DMAEO
ICLK2
IM1-
CE/WAIT-
BRAI
LS245
BR
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BDØ
DIR-
EQ
LS244
BIORQ-
BMREQ-
BRD-
BWR-
R13
330R
ICLK
FQ
07
ICLK2
BINT-
J4-30
J5
BRAI
(YELLOW)
LINK A
BUSAK-
BCLK
BM1-
BRESET-
IRESET-
PAL 10L8
(PORT DECODE)
*
CQ
DMA ENAB-
SIO ENAB-
SWITCH ENAB-
CTC1 ENAB
CTC2 ENAB-
CREG ENAB-
BACK-
BDSEL-
IIORQ-
PAL 14L4
DMA
SUPPORT
LOGIC
CP
MWAIT1
MWAIT2
DIR-
CE/WAIT-
BUS RD-
EACK-
IWAIT1-
244
IWAITO-
BWAIT-
IMREQ-
LS74
GV
WAIT STATE GENERATOR
* PDB = NETWORK BOARD
PD7 · DUAL SIO or TEST
† DMA OPTION DEVICES.
NOT FITTED.

MODIFICATION

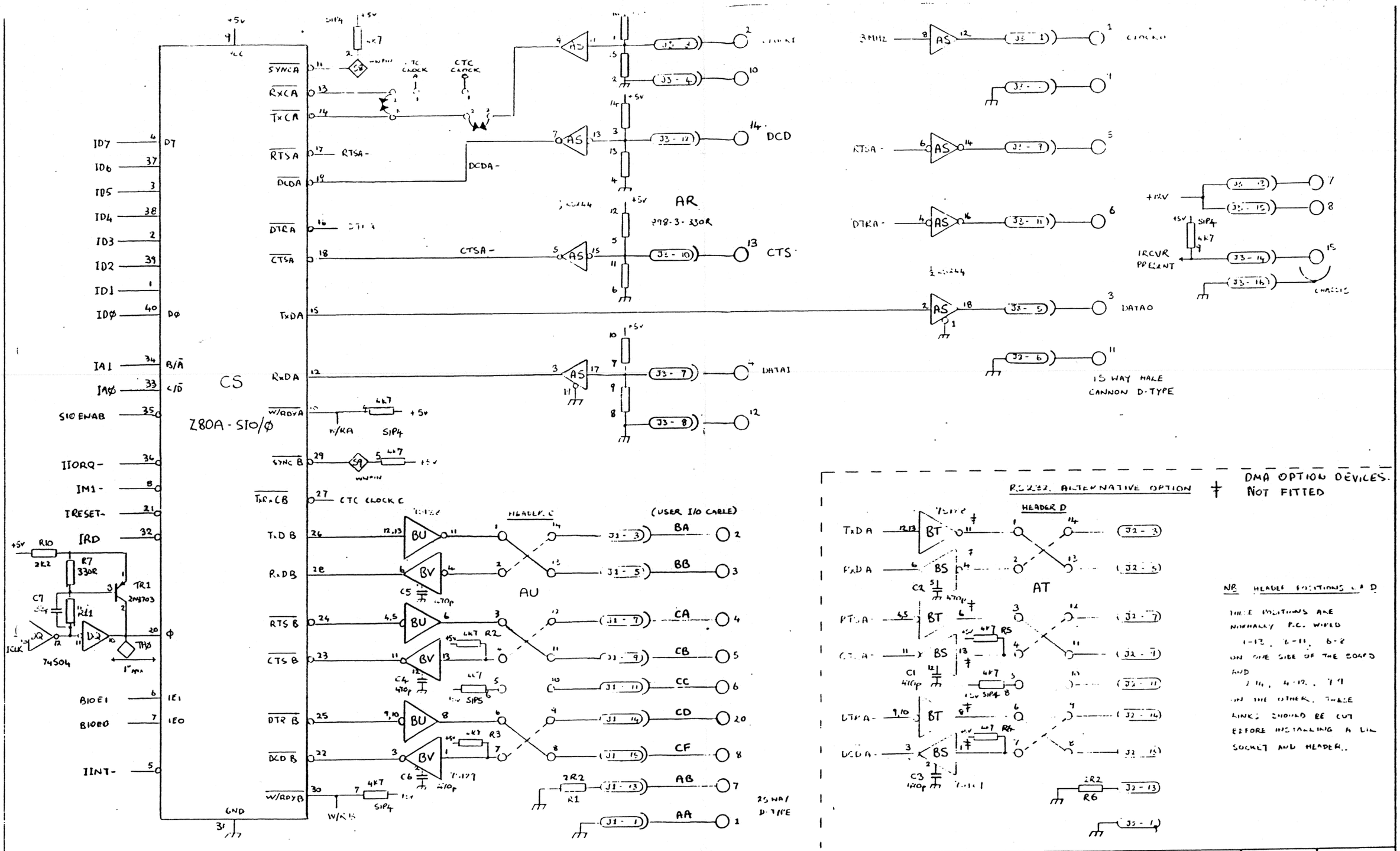
A	B	C	D	E	F	G	H	I
					6-3-81	7-4-81	17-?-81	30-3-82

Research Machines Ltd

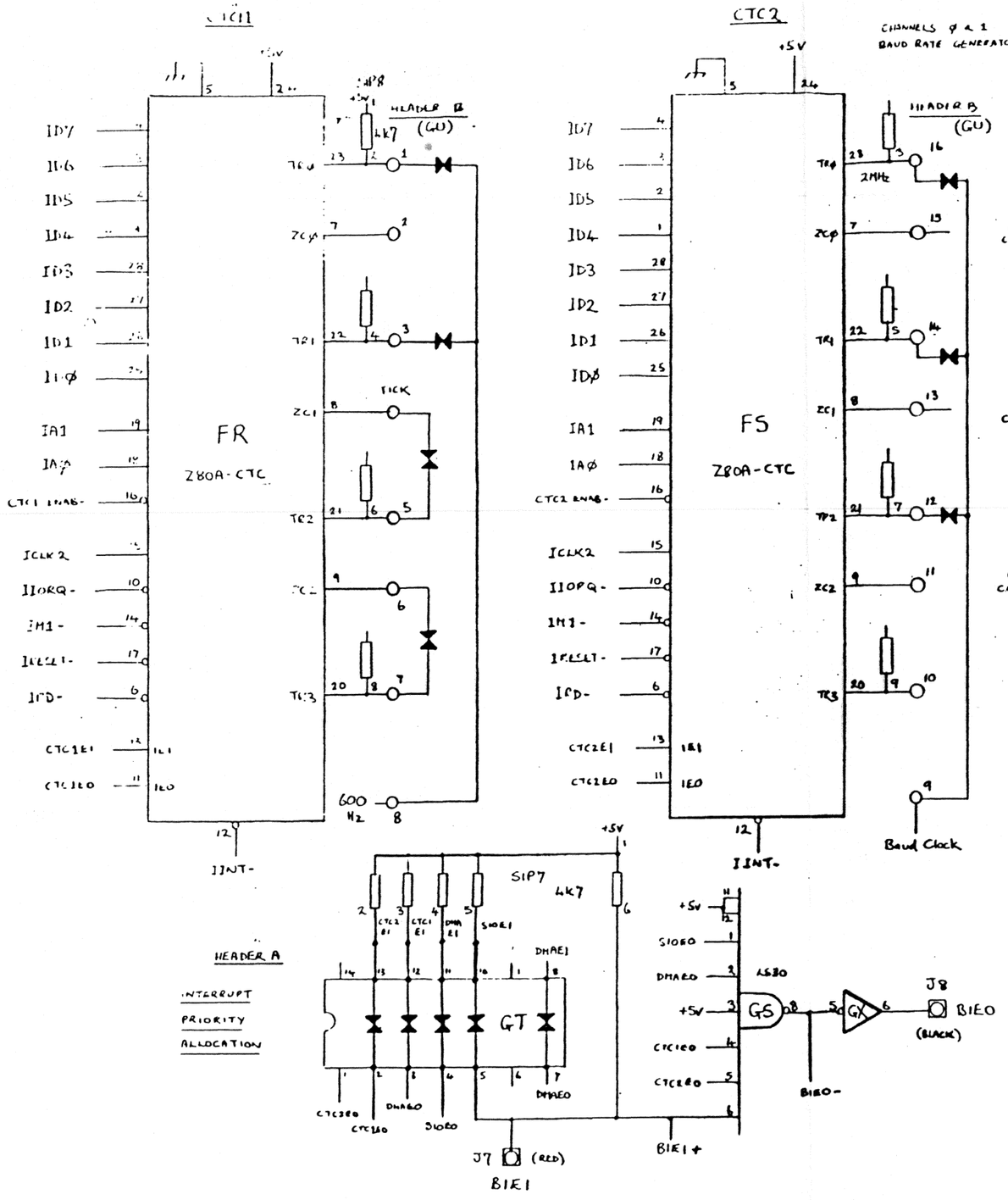
DATE	DRAWN BY	CHECKED BY
7-8-80	[signature]	

TITLE NETWORK / COMMUNICATIONS BOARD
BUS BUFFERING, CONTROL, DECODING & DMA

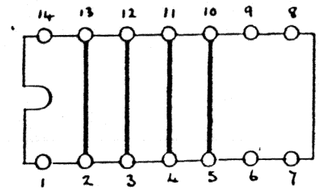
DRAWING No. 380Z - NET - 1



Research Machines Ltd	DATE	DRAWN BY	CHECKED BY
	12-12-80		
TITLE: NETWORK / COMMUNICATIONS BOARD SERIAL INTERFACE	DRAWING NO. 380Z - NET - 2		

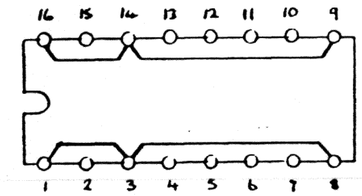


HEADER A — 11 PIN DIL — INTERRUPT PRIORITY ALLOCATION



PREWIRED. INTERRUPT PRIORITY MAY BE ALTERED

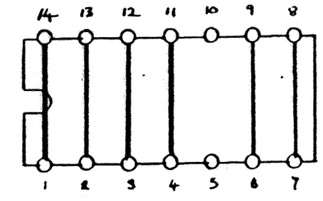
HEADER B — 16 PIN DIL — TIMING ROUTING



NOT NORMALLY INSTALLED

BREAK PREWIRED LINKS BEFORE FITTING SOCKET & HEADER

HEADER C — 14 PIN DIL — SIO-B RS232 USAGE

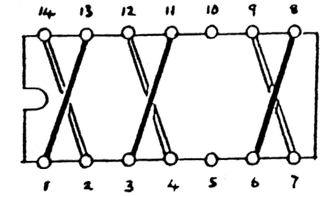


NOT NORMALLY INSTALLED

BREAK DATA & MODEM CONTROL SIGNALS IN DIL POSITION BEFORE FITTING SOCKET & HEADER

ABOVE HEADER SETS A SIO CHANNEL AS 'DCE'

HEADER D — 14 PIN DIL — SIO A RS232 USAGE



NOT NORMALLY INSTALLED

ONLY NECESSARY IF DATA & MODEM CONTROL SIGNAL WIRES HAVE BEEN CUT

ONLY USED IF CHANNEL A IS RS232

ABOVE HEADER SETS A SIO CHANNEL AS 'DTE'

MODIFICATION	
A	11-9-80
B	[illegible]
C	5-10-80
D	15-12-80
E	19-2-81
F	6-3-81
G	17-2-81
H	30-3-82

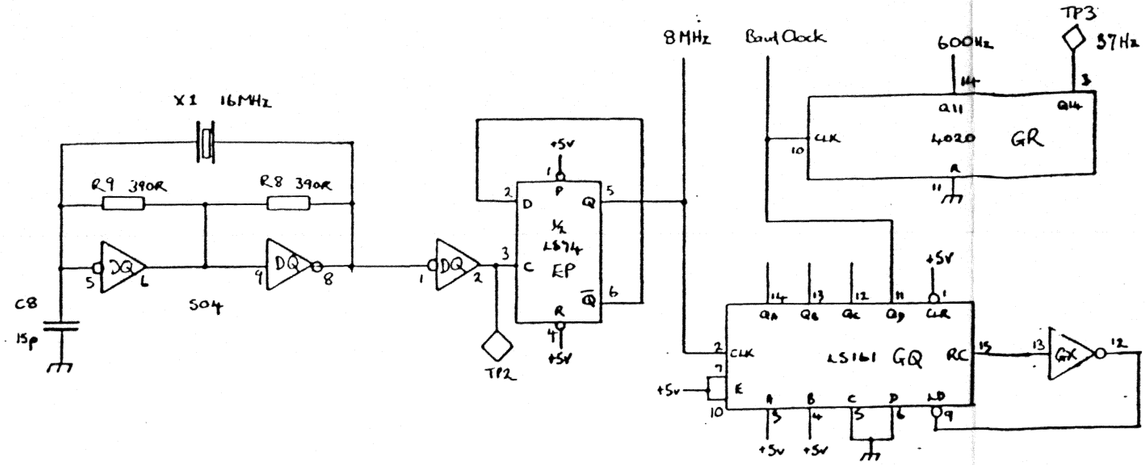
Research Machines Ltd

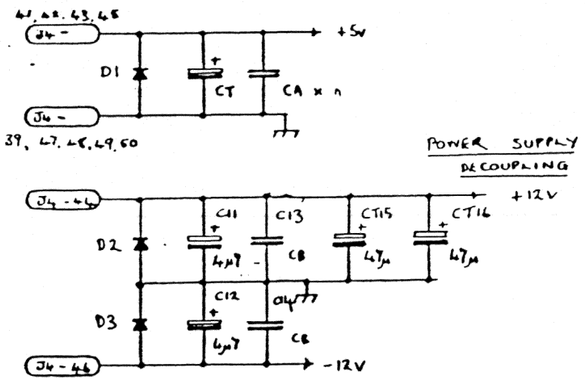
DATE	DRAWN BY	CHECKED BY
19-8-80	[signature]	

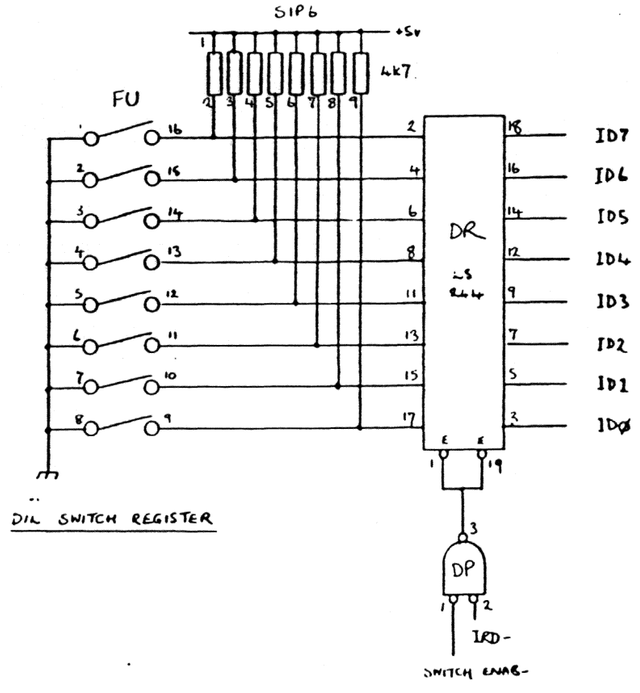
TITLE: NETWORK / COMMUNICATIONS BOARD
TIMING CONTROL

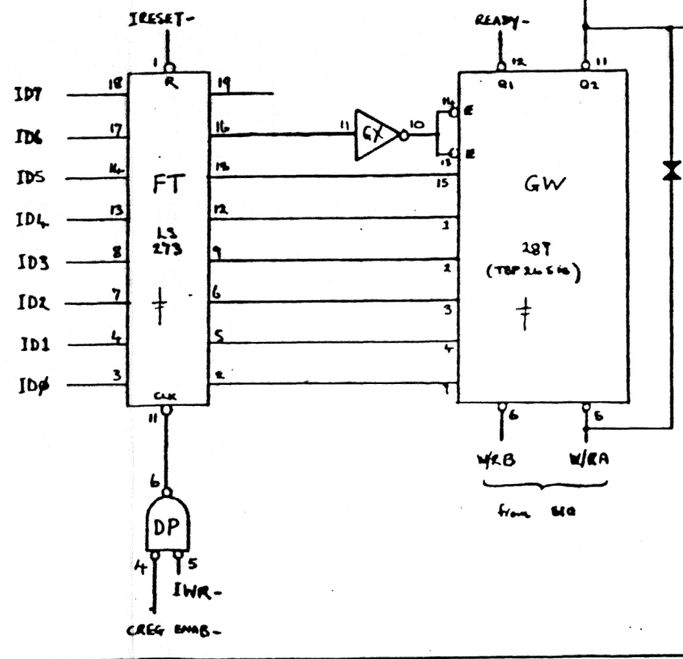
DRAWING NO. 380Z - NET - 3

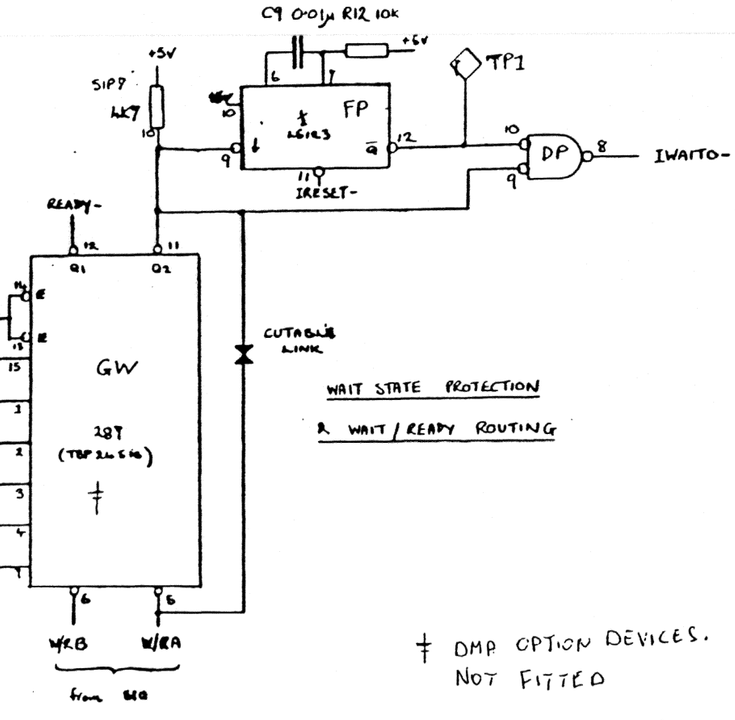
WP 1(H)











WAIT STATE PROTECTION

& WAIT / READY ROUTING

‡ DMP OPTION DEVICES. NOT FITTED

MODIFICATION		
A	17-8-81	
B	30-3-82	

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
17-8-81		

TITLE: NETWORK/COMMUNICATIONS BOARD MISCELLANEOUS FUNCTIONS 1

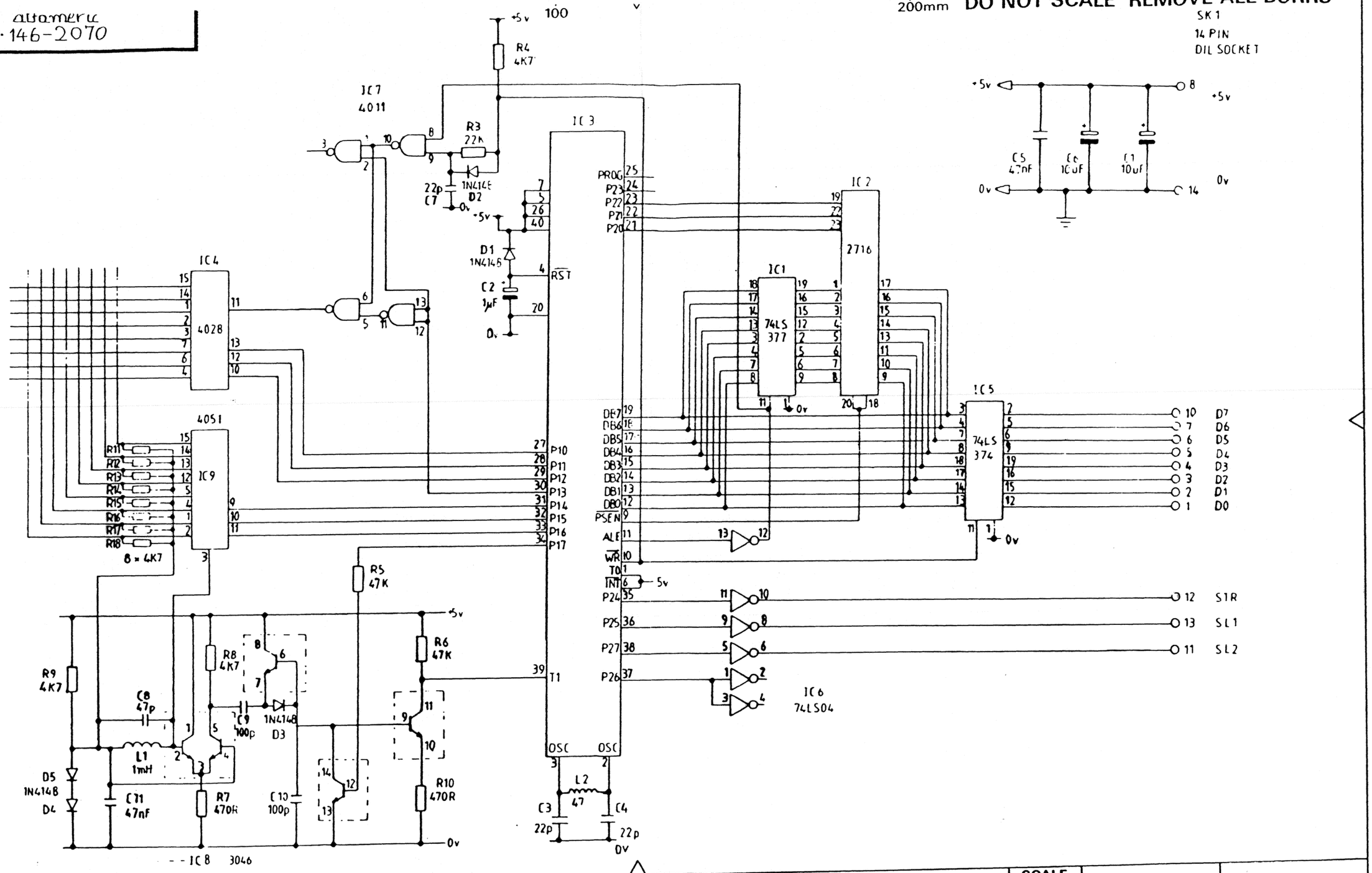
DRAWING NO. 380Z-NET-4

WP 1001

DRG. No. 146-2070

200mm DO NOT SCALE REMOVE ALL BURRS

SK1
14 PIN
DIL SOCKET

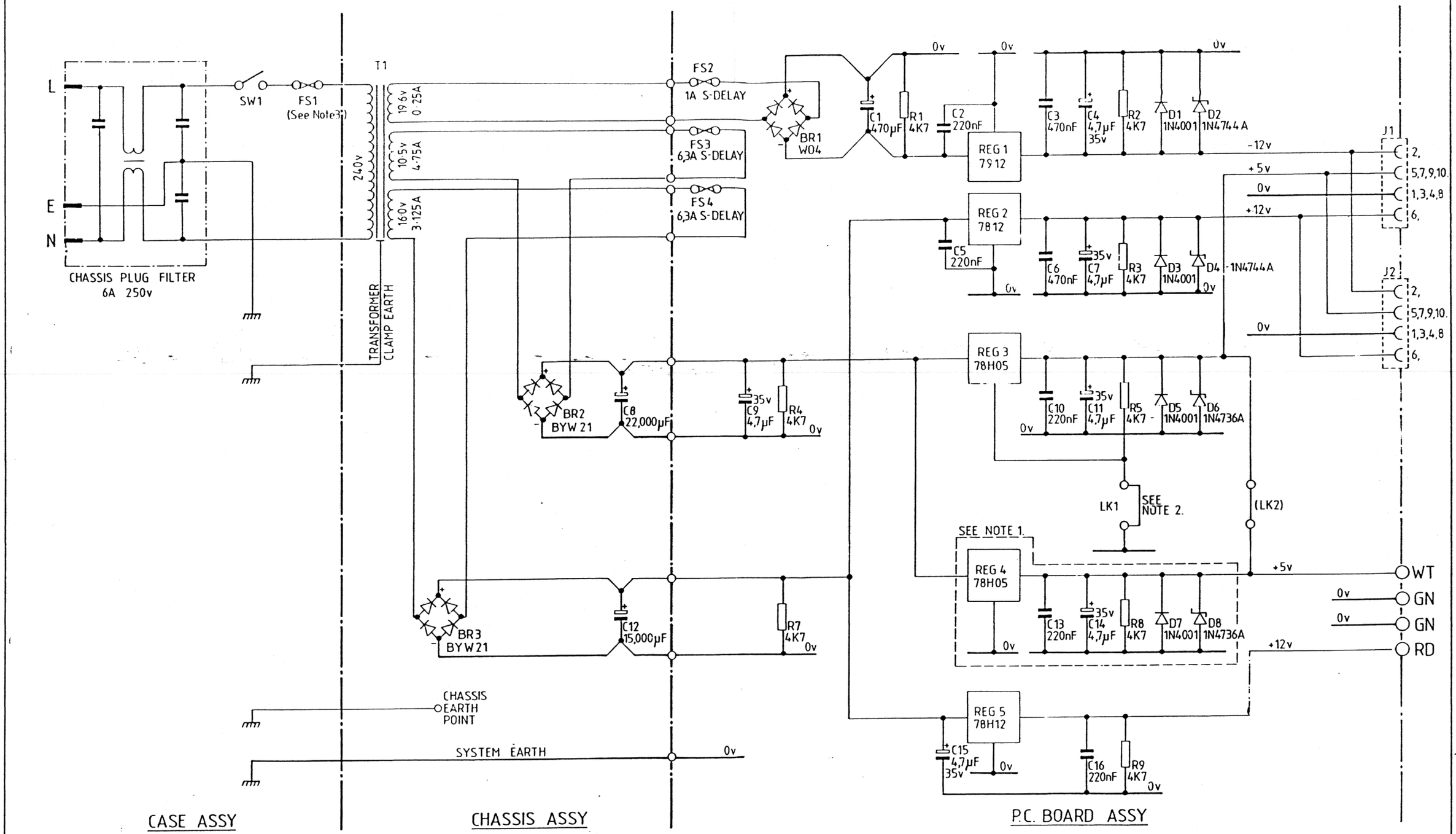


E.C.N.	UNLESS OTHERWISE STATED ASSUME:- ANGULAR TOLERANCE ± 1/2° WHOLE UNITS ± 0,5mm 1 DECIMAL PLACE ± 0,1mm GEOMETRICAL TOLERANCES SEE BS308 METRIC. THIRD ANGLE PROJECTION	RESEARCH MACHINES RESEARCH MACHINES LTD, Mill St. Oxford, OX2 0BW.	SCALE :
Date		TITLE: 380Z KEYBOARD	A3
Iss.			DRG. No.

DRN. | APRD. | DATE | CHKD.

AAROUE 4342/83

© 198 RESEARCH MACHINES LTD.



MODIFICATION	ECN	Date	Iss
rdrn		7·6·82	3

NOTES:
1. WHEN REG 4 & ASSOCIATED COMPONENTS ARE FITTED, CUT TRACK AT LK2.
2. LK1 MAY BE REPLACED WITH A RESISTOR (R6) TO INCREASE OUTPUT VOLTAGE OF REG 3.
3. FS1 TO BE LITTLEFUSE TYPE 314·001 OR APPROVED EQUIVALENT

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
7-6-82	DAG	

TITLE
380Z MODULAR POWER SUPPLY CCT. DIAG.

DRAWING NO.
D10875